ADM8511/X

USB/Fast Ethernet/HomePNA Controller

Communications

Never stop thinking.

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2000-06	Rev. 0.1: Draft product spec for review
2000-09	Rev. 1.0: Rearrange
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Page62/ 2000-12	Rev. 2.01: Appendix 5/item 7/item b/item ii/ TXER change to RXER
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2005-11-30	Minor change. Included Green package information

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1 General Description

The ADM8511/X, USB based chip set, provides desktop, notebook and computer peripheral with greater connectivity to ethernet and home network. In the meantime, the ADM8511/X also combines a low power and small package design which is ideal for power and space constrained by the environment. Then, it can reduce the external component BOM cost to a minimum. The ADM8511X is the environmentally friendly “green” package version.

The ADM8511/X device combines a on-chip USB command&EP decoder used for USB interface through SIE (Series Interface Engine), FIFO controller with 24 K SRAM, 64 byte and 2 K byte buffers, 10/100 Mbit/s ethernet physical layer (PHY) and 1M / 10M HomePNA interface 1M8 / 10M8. The 10M HomePNA interface is MII which is the same as the ethernet MAC interface. The ADM8511/X is fully compliant with the IEEE 802.3 u and HomePNA (Home Phoneline Network Alliance) specification reversion 1.0.

The ADM8511/X is capable of providing an easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 12 Mbit/s belonging to a high speed USB device. The ADM8511/X supports all USB commands, 4 endpoints and suspend/resume function.

The ADM8511/X’s LAN PHY supports 100 Base TX (100 Mbit/s mode) and 10 Base T (10 Mbit/s mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24M SRAM for receiving buffer, especially for 100 Mbit/s. Through FIFO controller, data cannot communicate fluently between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The Lan PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8511/X chip set can be programmed MAC analysis and it provides MII interface for external PHY, such as 10M8 interface for 1 Mbit/s HomePNA. In the system application, it is essential that the EEPROM loads device ID and vendor ID automatically. So for ADM8511/X, serial interface is applied for EEPROM communication including read/write function. Furthermore, different system status are reported by some LED pins including transfer speed LEDSP (100 Mbit/s or 10 Mbit/s), Link status (LEDL) on network and transfer type LEDFD/COL) full- duplex or half-duplex or collision on network.

ADM8511/X is ideally suited for USB adapter and intelligent networked peripheral design. By fiber media, ADM8511/X can associate with fiber transceiver & PHY through MII interface to network in fiber network. In HomePAN application, ADM8511/X can provide 1M8 interface and 10M8 (MII interface)associated with external 1M&10M Home PHY for 1 Mbit/s & 10 Mbit/s network. ADM8511/X can’t apply only in LAN (Local Area Network) but also in WAN (Wide Area Network), such as xDSL, Cable Modem, and router, etc. In IA (Information Appliance) application, Set-Top box is an example of ADM8511/X application. ADM8511/X also provides serial interface for EEPROM storing default values, e.g. vendor ID, Product ID, etc.(EEPROM Access Program). Specially, ADM8511/X can be tested by test program (MFG) in the less time for mass productions of system board level. This chip provides low power 0.35 μm, 3.3 V/5 V I/Otolerance, and 100 pin LQFP package

In software, ADM8511/X provides a fully software support, NDIS 5 driver, Linux driver, EEPROM burn-in program and MFG program. The NDIS 5 and Linux drivers are windows netware drivers. EEPROM burn-in program is convenient for customers to implement. The MFG program is a powerful tool in mass – production.

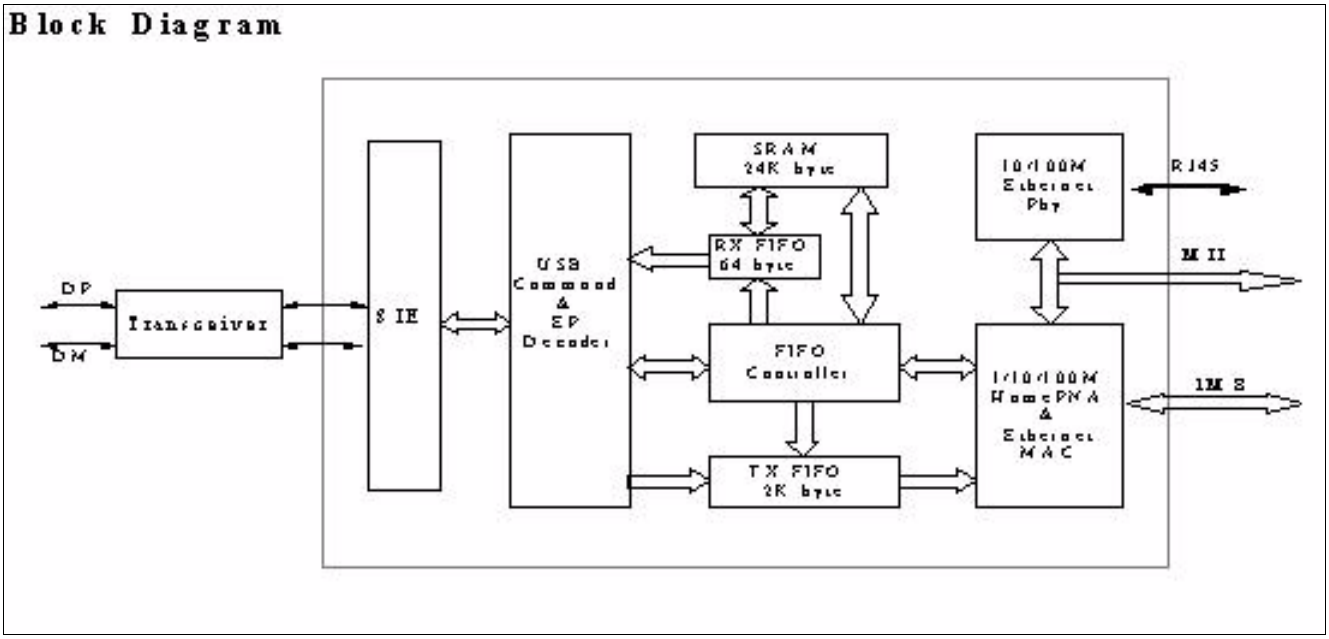


Figure 1 Block Diagram

1.1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM8511/X	ADM8511/X-CC-T-1	P-LQFP-100-1	Q67801H 26A101

1.2 Features

1.2.1 Industry Standard

- IEEE802.3 u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Supports for IEEE 802.3x flow control
- IEEE802.3 u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- USB specification 1.0 and 1.1 compliant

1.2.2 USB I/F

- Full-Speed USB Device
- Supports 1 USB configuration and 1 interface
- Supports all USB standard commands
- Supports two vendor specific commands
- Supports USB Suspend/Resume detection logic
- Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet

1.2.3 MAC/Phy

- Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using phy address 1
- Be programmed to isolate the internal PHY, the I/F to external PHY could be either IEEE 802.3 MII (10M8 for HomePNA 2.0). Supports configurable threshold for transmitting PAUSE frame
- Supports wakeup frame, link status change and magic packet wake-up
- Provides full-duplex operation on both 100 Mbit/s and 10 Mbit/s Ethernet modes
- Provides Auto-negotiation (NWAY) function of full/half duplex operation for both 10/100 Mbit/s
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
- Provides MAC and Transceiver loop-back modes for diagnostic
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

1.2.4 EEPROM I/F

- Provides serial interface for read/write 93C46 EEPROM
- Automatically load device ID, vendor ID from EEPROM after power-on reset

1.2.5 FIFO

- Supports internal 2 Kbytes SRAM for transmission
- Supports external 32 Kbytes SRAM or internal 24 Kbytes synchronous SRAM for receiving.
- Supports “receive 32 packets” or “receive 16 packets” queue in the receive buffer

1.2.6 LED Display

- Provides LED display
- LEDSP: Speed - 100 Mbit/s(on) or 10 Mbit/s(off)
- LEDL: Link (keeps on when link ok) or Active (will be blinking with 10 Hz)
- LEDFD/COL: FD (keeps on when in Full duplex mode) or Collision (will be blinking with 20 Hz when colliding)

1.2.7 Miscellaneous

- Supports 6 GPIO pins
- Provides 100-pin LQFP package
- 3.3 V power supply with 5 V/3.3 V I/O tolerance

1.2.8 LAN Driver Support

- Windows Networks: NDIS 5.0
- Linux

1.2.9 Utility

- EEPROM burn-in program

- MFG testing program

2 Interface Description

2.1 Pin Diagram

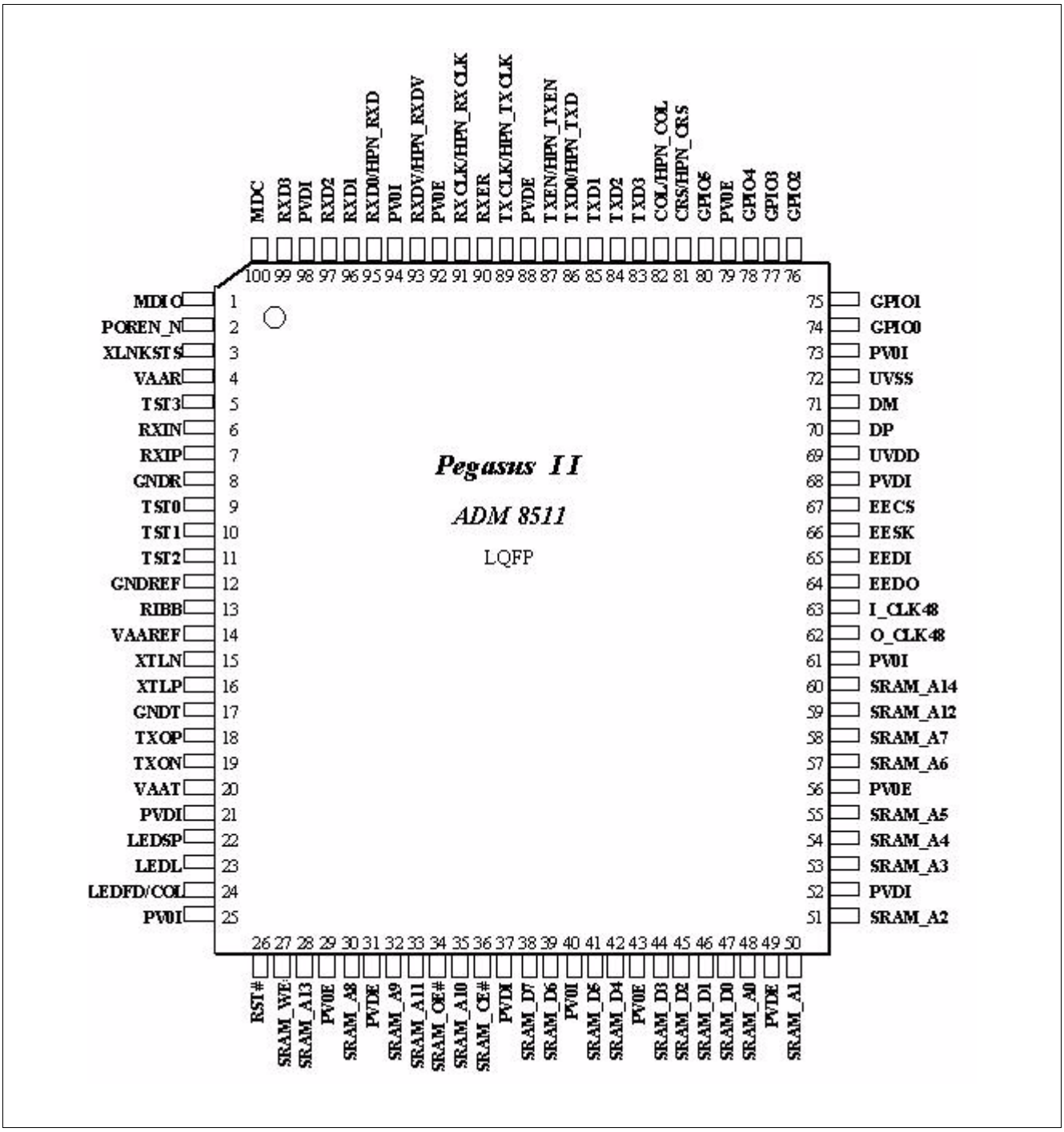


Figure 2 Pin Diagram

2.2 Pin Description

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Host Interface

Table 3 Host Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	I_CLK48	I		**48 MHz Clock Input from Crystal or Oscillator**
62	O_CLK48	O		**Output for Crystal**
26	RST#	I		**External Hardware Reset Input**
71	DM	I/O		**USB Data Minus Pin**
70	DP	I/O		**USB Data Plus Pin**

2.2.2 MII Interface

Program ADM8511/X as MAC-only mode, set 81_H[4:2]=001_B and 01_H bit 2 = 0

Table 4 MII Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
82	COL	I		**Collision Detected** This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
81	CRS	I		**Carrier Sense** This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
100	MDC	O		**Management Data Clock** Clock signal with a maximum rate of 2.5 MHz used to transfer management data for the external PMD on the MDIO pin.
1	MDIO	I/O		**Management Data I/O** Bi-directional signal used to transfer management information for the external PMD. Requires external 1.5 kΩ pull-up resistor.
91	RXCLK	I		**Receive Clock** A continuous clock that is recovered from the incoming data. During 100 Mbit/s operation RXCLK is 25 MHz, during 10 Mbit/s this is 2.5 MHz and during 1 Mbit/s operation this is 0.25 MHz.
95	RXD3	I		**Receive Data** This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit.
96	RXD2			
97	RXD1			
99	RXD0			

Table 4 MII Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
93	RXDV	I		**Receive Data Valid** This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data.
90	RXER	I		**Receive Error** This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted. If not used, it should be grounded, e.g. isolate internal phy and use external phy. However, if the external phy has RXER pin, the RXER of ADM8511/X should connect to this RXER of the external phy.
89	TXCLK	I		**Transmit Clock** A continuous clock sourced in the physical layer. During 100 Mbit/s operation this is 25 MHz ±100 ppm. During 10 Mbit/s operation this clock is 2.5 MHz ±100 ppm. During 1 Mbit/s operation this clock is 0.25 MHz ±100 ppm.
83	TXD3	O		**Transmit Data** This is a group of 4 data signals which are driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.
84	TXD2			
85	TXD1			
86	TXD0			
87	TXEN	O		**Transmit Enable** This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. Requires external pull-down resistor 4.7 kΩ if external phy is used
3	XLNKSTS	I		**Link Status Indication** External PHY reports link status information to system and level change trigger. Pull-down to low if external phy is used.

2.2.3 1M8 Interface

Program ADM8511/X as MAC-only mode, set 81_H[4:2]=001_B and 01_H bit 2 = 1

Table 5 1M8 Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
82	HPN_COL	I		**Collision** Indicates a collision was detected by the 1M8 PHY on the 1M8 wiring network.
81	HPN_CRS	I		**Carrier Sense** Indicates the 1M8 PHY is receiving a valid 1M8 signal from the wiring network.

Table 5 1M8 Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
91	HPN_RXCLK	I		**Receive Clock** Clock for RX_D.
95	HPN_RXD	I		**Receive Data** Data to the MAC is synchronously clocked by HPN_RXCLK.
93	HPN_RXDV	I		**Receive Data Valid** This indicates that the external physical unit is presenting recovered and decoded nibbles on the HPN_RXD and that HPN_RXCLK is synchronous to the recovered data.
89	HPN_TXCLK	I		**Transmit Clock** Clock for HPN_TXD.
86	HPN_TXD	O		**Transmit Data** Data to the PHY is synchronously clocked by HPN_TXCLK.
87	HPN_TXEN	O		**Transmit Enable** Transmits enable request from the MAC to begin sending data to the PHY.

2.2.4 Physical Interface

Table 6 Physical Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	XTLP	I		**Crystal inputs** To be connected to a 25 MHz crystal.
15	XTLN			
6	RXIN	I		The differential receives inputs of 100Base-TX or 10Base-T, these pins directly input from Magnetic.
7	RXIP			
18	TXOP	O		The differential Transmit outputs of 100Base-TX or 10Base-T, these pins directly output to Magnetic.
19	TXON			
13	RIBB	I		**Reference Bias Resistor** To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
9	TST0	I		**Test pin**
10	TST1			
11	TST2			
5	TST3			

2.2.5 LED Display

Table 7 LED Display

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
22	LEDSP	O		**LED Display for 100 Mbit/s or 10 Mbit/s Speed** Active low indicates 100Base-TX, active high indicates 10 BaseT.
23	LEDL	O		**LED Display for Link and Activity Status** Active low when link is established.
24	LEDFD/COL	O		**LED Display for Full Duplex or Collision Status** Active low indicates full duplex, high indicates collision in half duplex.

2.2.6 SRAM Interface

Table 8 SRAM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
48	SRAM_A14	O		**External SRAM Address Bus**
50	SRAM_A13			
51	SRAM_A12			
53	SRAM_A11			
54	SRAM_A10			
55	SRAM_A9			
57	SRAM_A8			
58	SRAM_A7			
30	SRAM_A6			
32	SRAM_A5			
35	SRAM_A4			
33	SRAM_A3			
59	SRAM_A2			
28	SRAM_A1			
60	SRAM_A0			
47	SRAM_D7	I/O	PD	**External SRAM Data Bus** Internal pull down
46	SRAM_D6			
45	SRAM_D5			
44	SRAM_D4			
42	SRAM_D3			
41	SRAM_D2			
39	SRAM_D1			
38	SRAM_D0			

Table 8 SRAM Interface (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
36	SRAM_CE#	O		**External SRAM Chip Enable**
34	SRAM_OE#	O		**External SRAM Output Enable**
27	SRAM_WE#	O		**External SRAM Write Enable**

2.2.7 EEPROM Interface

Table 9 EEPROM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	EECS	O		**EEPROM Chip Select** This enables the EEPROM during loading of the Ethernet configuration data.
65	EEDI	O		**EEPROM Data In** The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
64	EEDO	I		**EEPROM Data Out** The MAC will read the contents of the EEPROM serially through this pin.
66	EESK	O		**EEPROM Clock** After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM.

2.2.8 Miscellaneous

Table 10 Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
80	GPIO5	I/O		These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low
78	GPIO4			
77	GPIO3			
76	GPIO2			
75	GPIO1			
74	GPIO0			
2	POREN_N	I		**Internal Power On Reset Logic Enable** Default is enabled and internal pull - low. When external hardware reset is used, this pin should be connected to V_{cc} via 4.7 kΩ resistor.

2.2.9 Power Pins

Table 11 Power Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
21, 37, 52, 68, 98	PVDI	P		**3.3 V Power Supply for Core**
31, 49, 88	PVDE	P		**3.3 V Power Supply for Pads**
25, 40, 61, 73, 94	PV0I	P		**Ground for PVDI**
29, 43, 56, 79, 92	PV0E	P		**Ground for PVDE**
69	UVDD	P		**3.3 V Power Supply for USB Transceiver**
72	UVSS	P		**Ground for UVDD**
4	VAAR	P	P	**Analog Power Pins, 3.3 V**
14	VAAREF			
20	VAAT			
8	GNDR	P		**Analog Ground Pins**
12	GNDREF			
17	GNDT			

3 Function Description

3.1 USB Interface

USB is a likely solution when you want to use a computer to communicate with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced and standard peripheral. The benefits to USB are easy to use, fast and reliable data transfers, flexibility, low cost and power conservation.

3.1.1 SIE

SIE (Serial Interface Engine) is used to control USB communications and check USB protocol, and then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine

3.1.2 USB Command & EP Decoder

The detail description is in Appendix 4.

3.2 MAC Interface

3.2.1 MII

The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3 u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100 Mbit/s or 10 Mbit/s, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TX_EN is presented to the phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the phy synchronous to TX_CLK during the time that TX_EN is valid.

3.2.2 Adaptive Equalizer

The amplitude and phase distortions from cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The equalizer will tune itself automatically to any cable, compensating for the amplitude and phase distortion introduced by the cable.

3.2.3 LEDs

Individual LED output is available to indicate Speed, Duplex, Collision, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, the LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

3.2.4 Jabber and SQE

After the MAC transmitter exceeds the jabber timer, the transmit and loopback functions will be disable and COL signal gets asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

3.2.5 Auto Polarity

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy is able to detect the fact that either 8 NLPs (normal link pulse) or a burst of FLPs are inverted and automatically reverses the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

3.2.6 Auto-Negotiation

It provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determines common abilities, and configures joint operations. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10Base-T link integrity test sequence.

3.2.7 Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise, and fall times of the serial stream, can cause pulse-width distortion. This creates jitter and possibly increases in the bit error rates. Therefore, a DC restoration circuit is needed to compensate the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10Base-T, the baseline wander correction circuit is not required.

3.3 FIFO Controller

FIFO Controller in receive path is in charge of:

- Store received Ethernet packets to SRAM (internal 24 Kbyte or external 32 Kbyte) and total 32 (or 16) packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than 32 K (or 24 K for internal SRAM) bytes, the subsequent coming Ethernet packet will be discarded.
- FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller informs this, any USB access to bulk IN endpoint will return NAK. To maintain the data transfer on USB bus via bulk IN transfer must be continuously, thus a 64-byte internal RX FIFO is needed.
- If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

FIFO Controller in transmit path is in charge of:

- Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.
- Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packets are stored in TX FIFO or total packet size is more than 2 K bytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.

3.4 TX FIFO and RX FIFO

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2 Kbyte FIFO.

3.5 1/10/100 Ethernet/HomePNA MAC

The MAC controller takes in charge of:

- Generate CRC then transmit Ethernet packet.
- Check CRC for received packet CRC, filter the received packets.
- Polling PHY status.
- Magic packet detection.
- Automatically transmit PAUSE frame when received status meets the flow control criteria.
- Late collision transmit packets will be discarded.

3.6 10/100M Ethernet PHY

The internal Ethernet PHY is compliant to IEEE 802.3u 100Base-TX and IEEE802.3 10Base-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed. The internal PHY can be isolated by programming register offset $7B_H$, bit 1.

4 Registers Description

System Registers and Transceiver Registers.

4.1 System Registers

Table 12 Registers Address Space

Module	Base Address	End Address	Note
System Registers	0000 0000_H	0000 0081_H	

Table 13 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
EC0	Ethernet Control 0	00_H	29
EC1	Ethernet Control 1	01_H	30
EC2	Ethernet Control 2	02_H	31
Res0	Reserved 0	03_H	32
Res1	Reserved 1	04_H	32
Res2	Reserved 2	05_H	32
Res3	Reserved 3	06_H	32
Res4	Reserved 4	07_H	32
MC0	Multicast 0	08_H	32
MC1	Multicast 1	09_H	33
MC2	Multicast 2	$0A_H$	33
MC3	Multicast 3	$0B_H$	33
MC4	Multicast 4	$0C_H$	34
MC5	Multicast 5	$0D_H$	34
MC6	Multicast 6	$0E_H$	34
MC7	Multicast 7	$0F_H$	35
EID0	Ethernet ID 0	10_H	35
EID1	Ethernet ID 1	11_H	36
EID2	Ethernet ID 2	12_H	36
EID3	Ethernet ID 3	13_H	37
EID4	Ethernet ID 4	14_H	37
EID5	Ethernet ID 5	15_H	38
Res5	Reserved 5	16_H	38
Res6	Reserved 6	17_H	38
PTL	Pause Timer Low	18_H	39
Res7	Reserved 7	19_H	39
RPNBFC	Receive Packet Number Based Flow Control	$1A_H$	40
ORFBFC	Occupied Receive FIFO Based Flow Control	$1B_H$	40
EP1C	EP1 Control	$1C_H$	40
RXFC	RX FIFO Control	$1D_H$	41
BISTC	BIST Control	$1E_H$	41
Res8	Reserved 8	$1F_H$	42
EEPROMO	EEPROM Offset	20_H	42
EEPROMDL	EEPROM Data Low	21_H	43

Table 13 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
EEPROMDH	EEPROM Data High	22_H	**44**
EEPROMAC	EEPROM Access Control	23_H	**44**
Res9	Reserved 9	24_H	**45**
PHYA	PHY Address	25_H	**45**
PHYDL	PHY Data Low	26_H	**46**
PHYDH	PHY Data High	27_H	**46**
PHYAC	PHY Access Control	28_H	**47**
Res10	Reserved 10	29_H	**47**
USBBS	USB Bus Status	$2A_H$	**48**
TS1	Transmit Status 1	$2B_H$	**48**
TS2	Transmit Status 2	$2C_H$	**49**
RS	Receive Status	$2D_H$	**50**
RLPCH	Receive Lost Packet Count High	$2E_H$	**50**
RLPCL	Receive Lost Packet Count Low	$2F_H$	**51**
WUF0_M0	Wake-Up Frame 0 Mask 0	30_H	**51**
WUF0_M1	Wake-Up Frame 0 Mask 1	31_H	**51**
WUF0_M2	Wake-Up Frame 0 Mask 2	32_H	**51**
WUF0_M3	Wake-Up Frame 0 Mask 3	33_H	**51**
WUF0_M4	Wake-Up Frame 0 Mask 4	34_H	**51**
WUF0_M5	Wake-Up Frame 0 Mask 5	35_H	**51**
WUF0_M6	Wake-Up Frame 0 Mask 6	36_H	**51**
WUF0_M7	Wake-Up Frame 0 Mask 7	37_H	**51**
WUF0_M8	Wake-Up Frame 0 Mask 8	38_H	**51**
WUF0_M9	Wake-Up Frame 0 Mask 9	39_H	**51**
WUF0_M10	Wake-Up Frame 0 Mask 10	$3A_H$	**52**
WUF0_M11	Wake-Up Frame 0 Mask 11	$3B_H$	**52**
WUF0_M12	Wake-Up Frame 0 Mask 12	$3C_H$	**52**
WUF0_M13	Wake-Up Frame 0 Mask 13	$3D_H$	**52**
WUF0_M14	Wake-Up Frame 0 Mask 14	$3E_H$	**52**
WUF0_M15	Wake-Up Frame 0 Mask 15	$3F_H$	**52**
WUF0_O	Wake-Up Frame 0 Offset	40_H	**52**
WUF0_CRCL	Wake-Up Frame 0 CRC Low	41_H	**52**
WUF0_CRCH	Wake-Up Frame 0 CRC High	42_H	**53**
Res11	Reserved 11	43_H	**53**
Res12	Reserved12	44_H	**53**
Res13	Reserved13	45_H	**53**
Res14	Reserved14	46_H	**53**
Res15	Reserved15	47_H	**53**
WUF1_M0	Wake-Up Frame 1 Mask 0	48_H	**54**
WUF1_M1	Wake-Up Frame 1 Mask 1	49_H	**54**
WUF1_M2	Wake-Up Frame 1 Mask 2	50_H	**54**

Table 13 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WUF1_M3	Wake-Up Frame 1 Mask 3	51_H	54
WUF1_M4	Wake-Up Frame 1 Mask 4	52_H	54
WUF1_M5	Wake-Up Frame 1 Mask 5	53_H	54
WUF1_M6	Wake-Up Frame 1 Mask 6	54_H	54
WUF1_M7	Wake-Up Frame 1 Mask 7	55_H	54
WUF1_M8	Wake-Up Frame 1 Mask 8	56_H	54
WUF1_M9	Wake-Up Frame 1 Mask 9	57_H	54
WUF1_O	Wake-Up Frame 1 Offset	58_H	54
WUF1_CRCL	Wake-Up Frame 1 CRC Low	59_H	55
WUF1_CRCH	Wake-Up Frame 1 CRC High	$5A_H$	55
Res16	Reserved 16	$5B_H$	56
Res17	Reserved 17	$5C_H$	56
Res18	Reserved 18	$5D_H$	56
Res19	Reserved 19	$5E_H$	56
Res20	Reserved 20	$5F_H$	56
WUF2_M0	Wake-Up Frame 2 Mask 0	60_H	56
WUF2_M1	Wake-Up Frame 2 Mask 1	61_H	56
WUF2_M2	Wake-Up Frame 2 Mask 2	62_H	56
WUF2_M3	Wake-Up Frame 2 Mask 3	63_H	57
WUF2_M4	Wake-Up Frame 2 Mask 4	64_H	57
WUF2_M5	Wake-Up Frame 2 Mask 5	65_H	57
WUF2_M6	Wake-Up Frame 2 Mask 6	66_H	57
WUF2_M7	Wake-Up Frame 2 Mask 7	67_H	57
WUF2_M8	Wake-Up Frame 2 Mask 8	68_H	57
WUF2_M9	Wake-Up Frame 2 Mask 9	69_H	57
WUF2_M10	Wake-Up Frame 2 Mask 10	$6A_H$	57
WUF2_M11	Wake-Up Frame 2 Mask 11	$6B_H$	57
WUF2_M12	Wake-Up Frame 2 Mask 12	$6C_H$	57
WUF2_M13	Wake-Up Frame 2 Mask 13	$6D_H$	57
WUF2_M14	Wake-Up Frame 2 Mask 14	$6E_H$	57
WUF2_M15	Wake-Up Frame 2 Mask 15	$6F_H$	57
WUF2_O	Wake-Up Frame 2 Offset	70_H	57
WUF2_CRCL	Wake-Up Frame 2 CRC Low	71_H	57
WUF2_CRCH	Wake-Up Frame 2 CRC High	72_H	58
Res21	Reserved 21	73_H	58
Res22	Reserved 22	74_H	58
Res23	Reserved 23	75_H	58
Res24	Reserved 24	76_H	58
Res25	Reserved 25	77_H	58
WUC	Wake-Up Control	78_H	59
Res26	Reserved 26	79_H	59

Table 13 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WUS	Wake-Up Status	$7A_H$	60
IPHYC	Internal PHY Control	$7B_H$	60
GPIO54	GPIO 5:4	$7C_H$	61
Res27	Reserved 27	$7D_H$	61
GPIO10	GPIO 1:0	$7E_H$	62
GPIO32	GPIO 3:2	$7F_H$	62
TR	TEST Register	80_H	63
TM	Test Mode	81_H	64

The register is addressed wordwise.

Table 14 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared

Table 14 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 15 Registers Clock Domains

Clock Short Name	Description

4.1.1

Ethernet Control 0

EC0	Offset	Reset Value
Ethernet Control 0	**00_H**	**09_H**

7	6	5	4	3	2	1	0
TXE	**RXE**	**RXFCE**	**WOE**	**RXSA**	**SBO**	**RXMA**	**RXCS**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TXE	7	rw	**Enable Ethernet Transmission** tx_en
RXE	6		**Enable Ethernet Receive** rx_en
RXFCE	5		**Enable Receive Pause Frame** rx_flowctl_en
WOE	4		**Enable Wake-On-LAN Mode** wakeon_en
RXSA	3		**Enable Status Append at the End of Received Packet** rxstatus_append

Field	Bits	Type	Description
SBO	2	rw	**Stop Back Off** 0_B , back-off counter isn't affected by carrier. 1_B , back-off counter stops when carrier is active and resumes when carrier is dropped.
RXMA	1		**Receive All Multicast Packet** rx_multicast_all
RXCS	0		**Include CRC in Receive Packet** rx_crc_sent

Ethernet Control 1

EC1 **Offset** **Reset Value**

Ethernet Control 1 **01_H** **00_H**

7	6	5	4	3	2	1	0
Res	**DH**	**FD**	**10M**	**RM**	**HM**	Res	
ro	rw	rw	rw	rw	rw	ro	

Field	Bits	Type	Description
Res	7	ro	**Reserved**
DH	6	rw	**Delay Home** 0_B , all data is received after HPN_CRS asserts 1_B , 1 bit data is dropped after HPN_CRS asserts
FD	5		**Full Duplex** 0_B , half-duplex mode 1_B , full-duplex mode
10M	4		**10Mode** 0_B , 10Base-T mode 1_B , 100Base-T mode
RM	3		**Reset MAC** Reset MAC, After write 1, HW will clear this bit after MAC resets.
HM	2		**Homelan Mode** 0_B , MII I/F to external PHY 1_B , 1M8 I/F to external PHY
Res	1:0	ro	**Reserved**

Ethernet Control 2

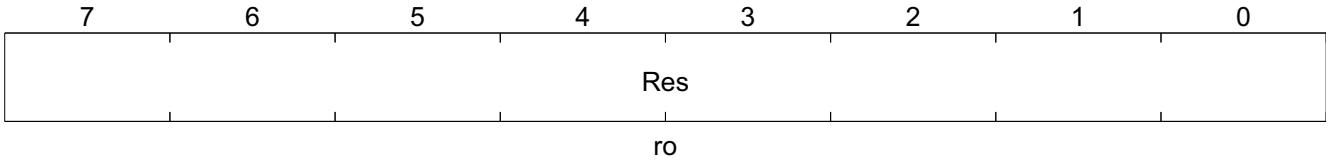
EC2	Offset	Reset Value
Ethernet Control 2	02_H	00_H

7	6	5	4	3	2	1	0
Res		LES	EWED	LB	PR	RBP	E3RC
ro		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
LES	5	rw	**Load EEPROM Start** When this bit is written with 1, HW will start to load EEPROM.
EWED	4		**EEPROM Write Enable/Disable** 0_B , EEPROM writes enable/disable command 1_B , EEPROM writes command
LB	3		**Loop Back** Enables MAC in a loop back mode
PR	2		**Promiscuous** 0_B , receives packets which pass the address filter 1_B , receives any packet
RBP	1		rx_bad_pkt 0_B , filters all bad packets 1_B , receives bad packets which pass the address filter
E3RC	0		Ep3_rd_clr/ 0_B , Access EP3, no effect to those registers. 1_B , Once EP3 is accessed those registers (2B-2F, 7A) will be cleared.

Reserved 0

Res0	Offset	Reset Value
Reserved 0	**03_H**	**00_H**



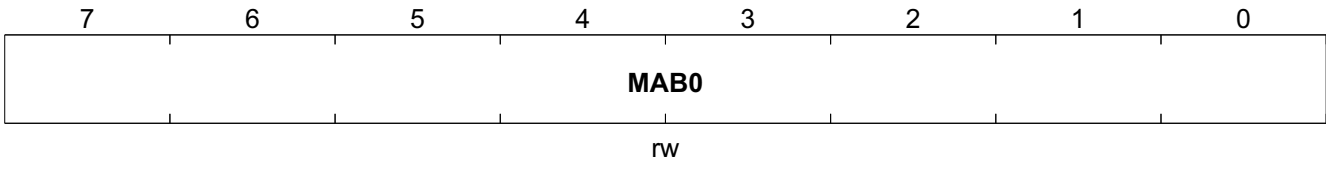
Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Table 16 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res1	Reserved 1	04_H	
Res2	Reserved 2	05_H	
Res3	Reserved 3	06_H	
Res4	Reserved 4	07_H	

Multicast 0

MC0	Offset	Reset Value
Multicast 0	**08_H**	**00_H**

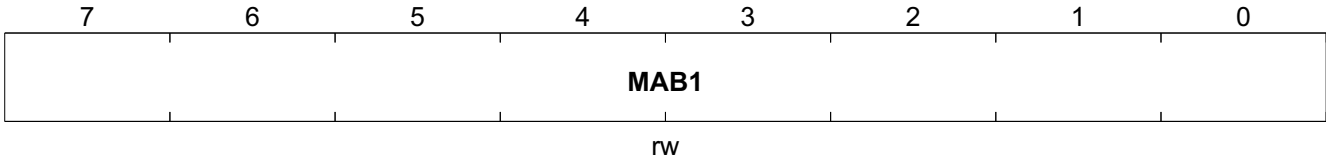


Field	Bits	Type	Description
MAB0	7:0	rw	**Multicast Address Byte 7:0**

Multicast 1

MC1 **Offset** **Reset Value**

Multicast 1 **09_H** **00_H**

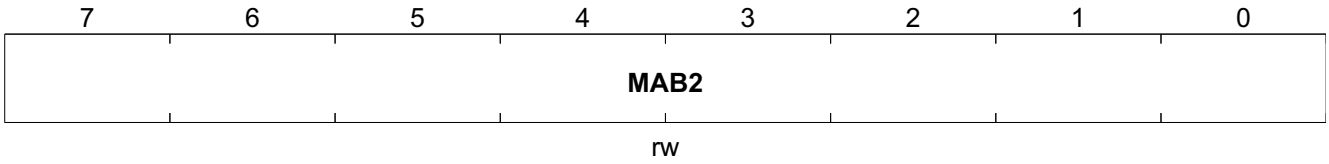


Field	Bits	Type	Description
MAB1	7:0	rw	**Multicast Address Byte 15:8**

Multicast 2

MC2 **Offset** **Reset Value**

Multicast 2 **$0A_H$** **00_H**

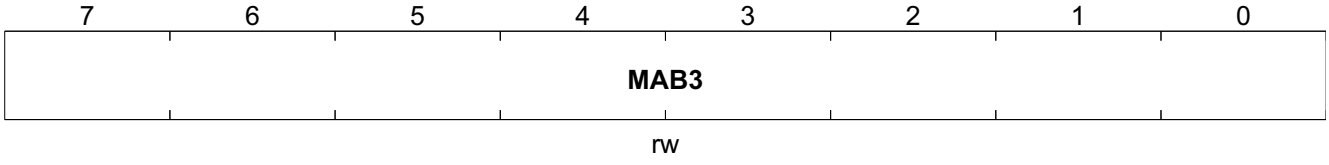


Field	Bits	Type	Description
MAB2	7:0	rw	**Multicast Address Byte 23:16**

Multicast 3

MC3 **Offset** **Reset Value**

Multicast 3 **$0B_H$** **00_H**



Field	Bits	Type	Description
MAB3	7:0	rw	**Multicast Address Byte 31:24**

Multicast 4

MC4 **Offset** **Reset Value**

Multicast 4 **$0C_H$** **00_H**

7	6	5	4	3	2	1	0
MAB4							
rw							

Field	Bits	Type	Description
MAB4	7:0	rw	**Multicast Address Byte 39:32**

Multicast 5

MC5 **Offset** **Reset Value**

Multicast 5 **$0D_H$** **00_H**

7	6	5	4	3	2	1	0
MAB5							
rw							

Field	Bits	Type	Description
MAB5	7:0	rw	**Multicast Address Byte 47:40**

Multicast 6

MC6 **Offset** **Reset Value**

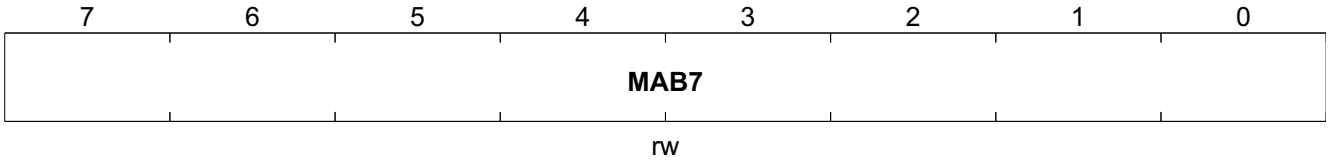
Multicast 6 **$0E_H$** **00_H**

7	6	5	4	3	2	1	0
MAB6							
rw							

Field	Bits	Type	Description
MAB6	7:0	rw	**Multicast Address Byte 55:48**

Multicast 7

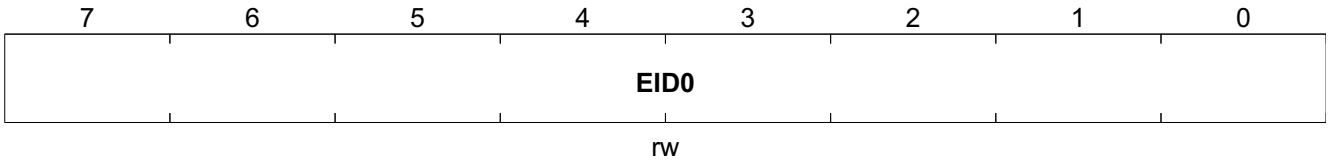
MC7	Offset	Reset Value
Multicast 7	$0F_H$	00_H



Field	Bits	Type	Description
MAB7	7:0	rw	**Multicast Address Byte 63:56**

Ethernet ID 0

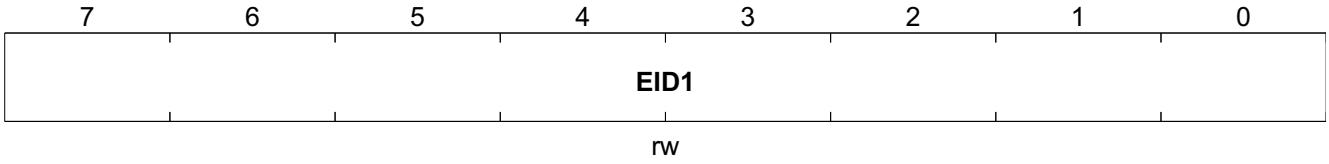
EID0	Offset	Reset Value
Ethernet ID 0	10_H	00_H



Field	Bits	Type	Description
EID0	7:0	rw	**Ethernet ID 0** The 1st byte of ethernet ID is automatically loaded from EEPROM after HW reset.

Ethernet ID 1

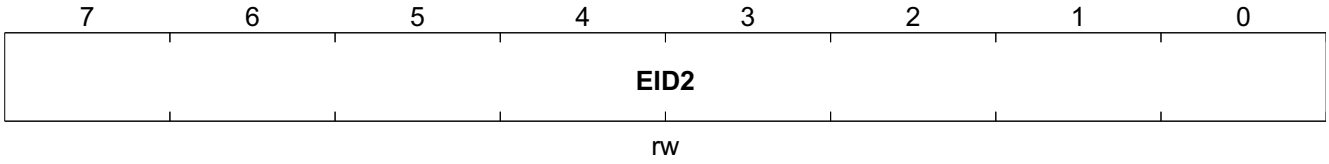
EID1	Offset	Reset Value
Ethernet ID 1	11_H	00_H



Field	Bits	Type	Description
EID1	7:0	rw	**Ethernet ID 1** The 2nd byte of ethernet ID.

Ethernet ID 2

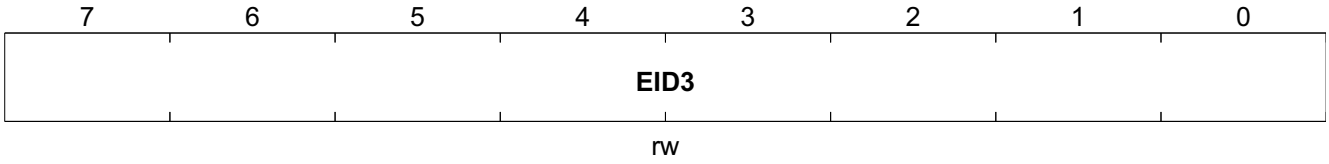
EID2	Offset	Reset Value
Ethernet ID 2	12_H	00_H



Field	Bits	Type	Description
EID2	7:0	rw	**Ethernet ID 2** The 3rd byte of ethernet ID.

Ethernet ID 3

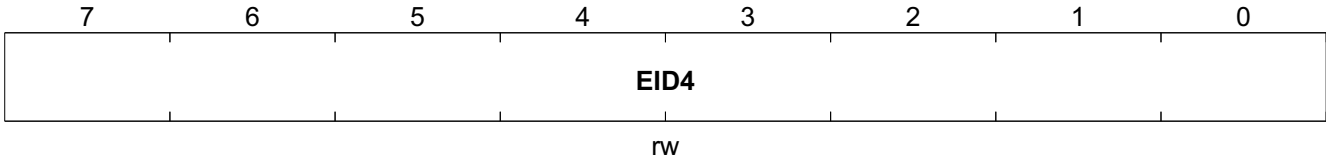
EID3	Offset	Reset Value
Ethernet ID 3	13_H	00_H



Field	Bits	Type	Description
EID3	7:0	rw	**Ethernet ID 3** The 4th byte of ethernet ID.

Ethernet ID 4

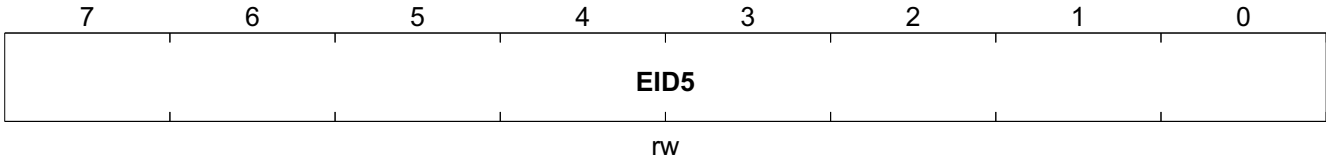
EID4	Offset	Reset Value
Ethernet ID 4	14_H	00_H



Field	Bits	Type	Description
EID4	7:0	rw	**Ethernet ID 4** The 5th byte of ethernet ID.

Ethernet ID 5

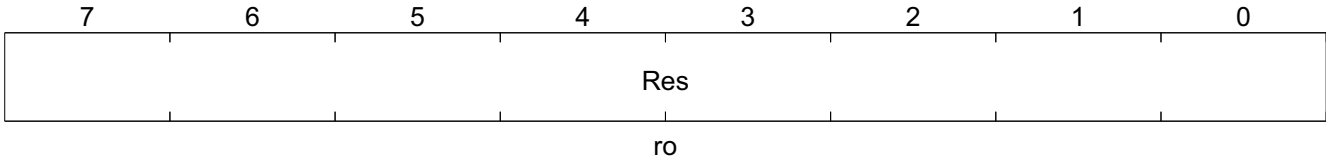
EID5	Offset	Reset Value
Ethernet ID 5	15_H	00_H



Field	Bits	Type	Description
EID5	7:0	rw	**Ethernet ID 5** The 6th byte of ethernet ID.

Reserved 5

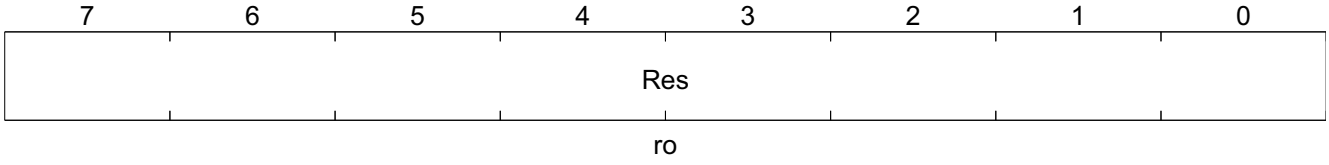
Res5	Offset	Reset Value
Reserved 5	16_H	00_H



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Reserved 6

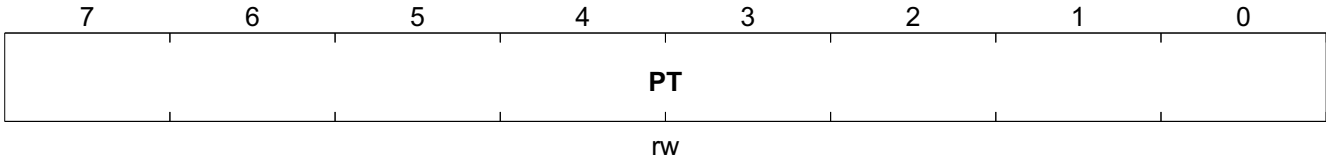
Res6	Offset	Reset Value
Reserved 6	17_H	00_H



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Pause Timer Low

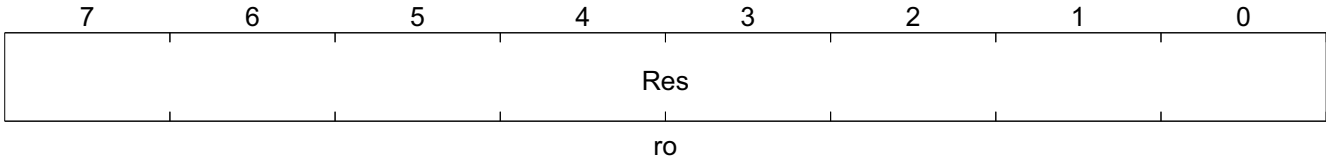
PTL	Offset	Reset Value
Pause Timer Low	18_H	00_H



Field	Bits	Type	Description
PT	7:0	rw	**Pause Timer** The [11:4] of pause time in the PAUSE frame.

Reserved 7

Res7	Offset	Reset Value
Reserved 7	19_H	00_H



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Receive Packet Number Based Flow Control

RPNBFC	Offset	Reset Value
Receive Packet Number Based Flow Control	$1A_H$	00_H

7	6	5	4	3	2	1	0
Res	PN						FP
ro	rw						rw

Field	Bits	Type	Description
Res	7	ro	**Reserved**
PN	6:1	rw	**Packet Number** This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
FP	0	rw	**Flow Control Packet** Enabled pause frame transmission bases on received packet number.

Occupied Receive FIFO Based Flow Control

ORFBFC	Offset	Reset Value
Occupied Receive FIFO Based Flow Control	$1B_H$	00_H

7	6	5	4	3	2	1	0
Res	RXS						FRXS
ro	rw						rw

Field	Bits	Type	Description
Res	7	ro	**Reserved**
RXS	6:1	rw	**RX Size** This field specifies the Kbyte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field =2, as receive FIFO is occupied more than or equal to 2 Kbyte, the PAUSE frame is transmitted.
FRXS	0		**Flow Control RX Size** Enabled pause frame transmission bases on occupied receive FIFO size.

EP1 Control

EP1C **Offset** **Reset Value**
EP1 Control **$1C_H$** **00_H**

7	6	5	4	3	2	1	0
EPSE	**TIA**		**TIB**				
rw	rw		rw				

Field	Bits	Type	Description
EPSE	7	rw	**EP1 Send0 Enable** 0_B , Disables EP1 send 1-byte 00 function 1_B , Enables EP1 send 1-byte 00 when more than frame_interval's NAK is received
TIA	6:5	rw	**Test Interval A** This value is used for internal test mode.
TIB	4:0	rw	**Test Interval B** This value is used for internal test mode.

RX FIFO Control

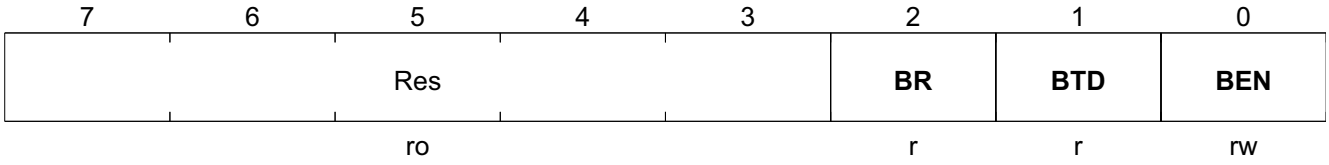
RXFC **Offset** **Reset Value**
RX FIFO Control **$1D_H$** **00_H**

7	6	5	4	3	2	1	0
Res						**ESE**	**R32P**
ro						rw	rw

Field	Bits	Type	Description
Res	7:2	ro	**Reserved**
ESE	1	rw	**External SRAM Enable** 0_B , Supports internal 24 Kbyte SRAM 1_B , Supports external 32 Kbyte SRAM
R32P	0		**Receive 32 Packets** 0_B , Supports maximum 16 packets in receive FIFO 1_B , Supports maximum 32 packets in receive FIFO

BIST Control

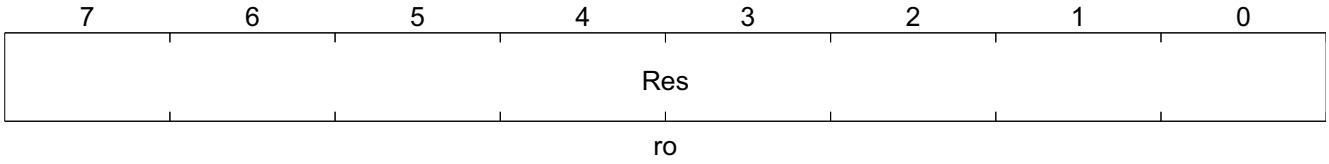
BISTC **Offset** **Reset Value**
BIST Control **$1E_H$** **01_H**



Field	Bits	Type	Description
Res	7:3	ro	**Reserved**
BR	2	r	**BIST Result** This bit indicates the bist result and is valid when “bist_test_done” is ‘1’. This bit also reflects the value of “pass_or_fail” signal in BIST module. 0_B , Fail 1_B , Pass
BTD	1	r	**BIST Test Done** This bit indicates the completion of bist. The bist completes if this bit is ‘1’. This bit also reflects the value of “test_done” signal in BIST module.
BEN	0	rw	**BIST Enable** This bit enables the BIST function and also drives the “reset” signal in BIST module. 0_B , Enable BIST function 1_B , Disable BIST function

Reserved 8

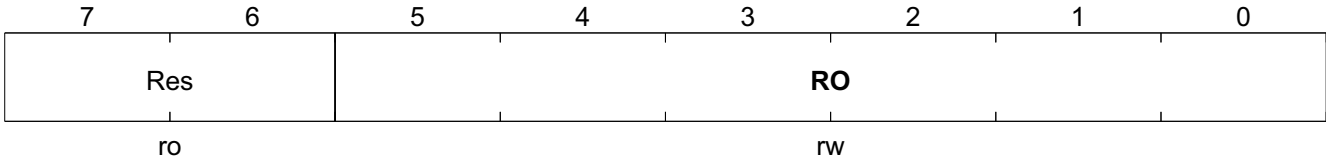
Res8	Offset	Reset Value
Reserved 8	**$1F_H$**	**00_H**



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

EEPROM Offset

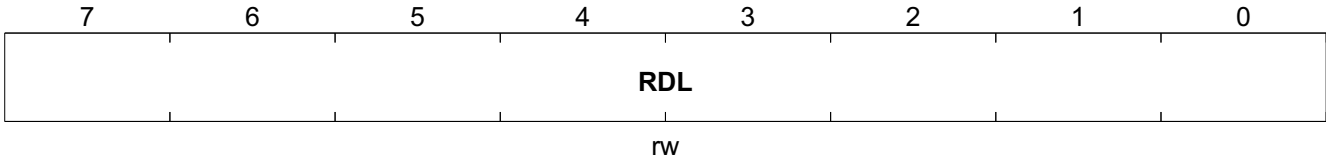
EEPROMO	Offset	Reset Value
EEPROM Offset	**20_H**	**00_H**



Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
RO	5:0	rw	**ROM Offset** SW sets this register when access to EEPROM.

EEPROM Data Low

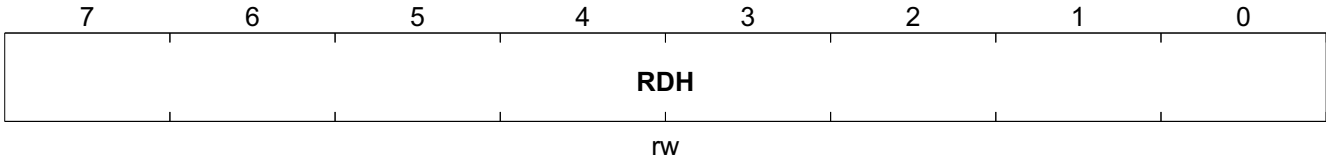
EEPROMDL	Offset	Reset Value
EEPROM Data Low	21_H	00_H



Field	Bits	Type	Description
RDL	7:0	rw	**ROM Data Low** SW sets this register when writes to EEPROM. HW sets this register when read data from EEPROM.

EEPROM Data High

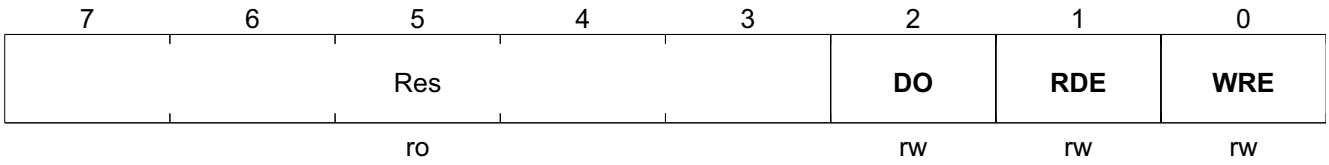
EEPROMDH	Offset	Reset Value
EEPROM Data High	22_H	00_H



Field	Bits	Type	Description
RDH	7:0	rw	**ROM Data High** SW sets this register when writes to EEPROM. HW sets this register when reads data from EEPROM.

EEPROM Access Control

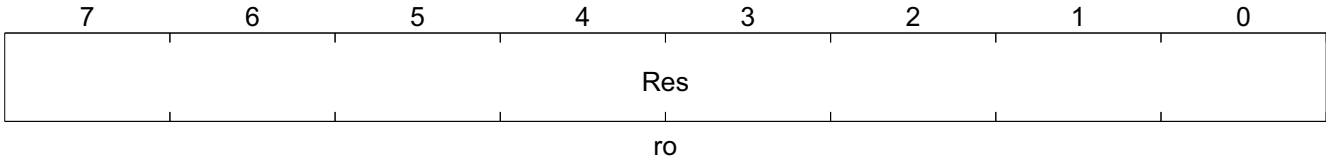
EEPROMAC	Offset	Reset Value
EEPROM Access Control	23_H	00_H



Field	Bits	Type	Description
Res	7:3	ro	**Reserved**
DO	2	rw	**Done** Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM.
RDE	1		**Read Access to EEPROM** Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
WRE	0		**Write Access to EEPROM** Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

Reserved 9

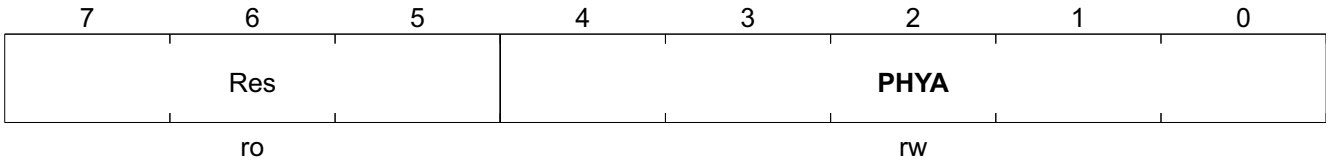
Res9	Offset	Reset Value
Reserved 9	**24_H**	**00_H**



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

PHY Address

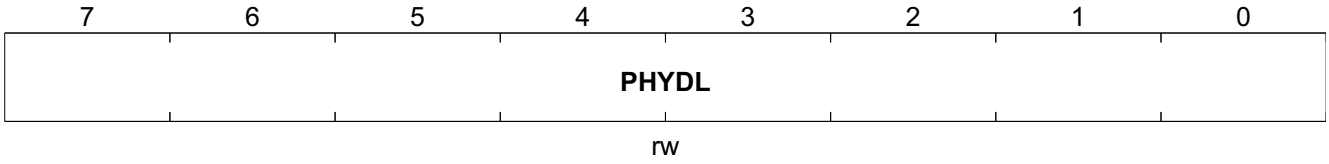
PHYA	Offset	Reset Value
PHY Address	**25_H**	**00_H**



Field	Bits	Type	Description
Res	7:5	ro	**Reserved**
PHYA	4:0	rw	**MII PHY Address**

PHY Data Low

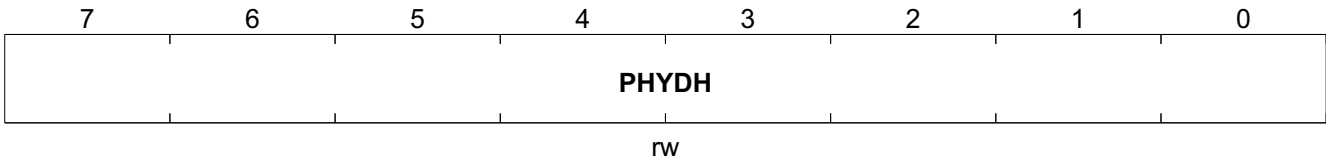
PHYDL	Offset	Reset Value
PHY Data Low	26_H	00_H



Field	Bits	Type	Description
PHYDL	7:0	rw	**PHY Data Low** SW set this register when write to phy registers. HW set this register when read data from PHY register.

PHY Data High

PHYDH	Offset	Reset Value
PHY Data High	27_H	00_H



Field	Bits	Type	Description
PHYDH	7:0	rw	**PHY Data High** SW set this register when write to phy registers. HW set this register when read data from PHY register.

PHY Access Control

PHYAC **Offset** **Reset Value**

PHY Access Control **28_H** **00_H**

7	6	5	4	3	2	1	0
DO	**RDP**	**WRP**	**PRA**				
rw	rw	rw	rw				

Field	Bits	Type	Description
DO	7	rw	**Done** Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
RDP	6		**Read Access to PHY Register** Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
WRP	5		**Write Access to PHY Register** Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
PRA	4:0		**PHY Register Address**

Reserved 10

Res10 **Offset** **Reset Value**

Reserved 10 **29_H** **00_H**

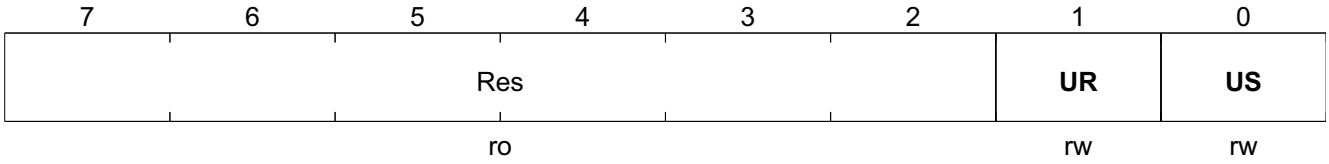
7	6	5	4	3	2	1	0
Res							
ro							

Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

USB Bus Status

USBBS **Offset** **Reset Value**

USB Bus Status **$2A_H$** **00_H**

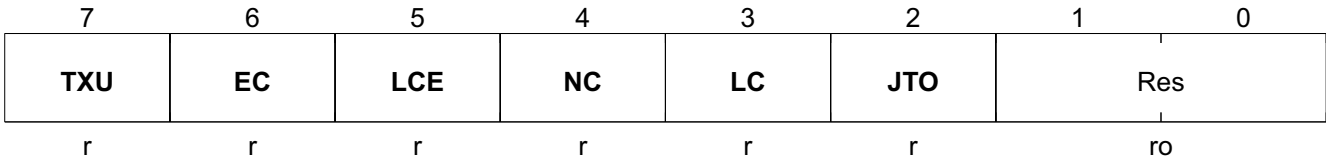


Field	Bits	Type	Description
Res	7:2	ro	**Reserved**
UR	1	rw	**USB Bus in Resume State** Set by HW to indicate usb bus in resumed state. Clear by SW read this register.
US	0		**USB Bus in Suspend State** Set by HW to indicate usb bus in suspended state. Clear by SW read this register.

Transmit Status 1

TS1 **Offset** **Reset Value**

Transmit Status 1 **$2B_H$** **00_H**



Field	Bits	Type	Description
TXU	7	r	**TX Underrun Error** Set by HW to indicate tx underrun error. Clear this register by SW Read or after EP3 is accessed.
EC	6		**Excessive Collision** Set by HW to indicate excessive collision. Clear this register by SW Read or after EP3 is accessed.
LCE	5		**Late Collision Error** Set by HW to indicate late collision error. Clear this register by SW Read or after EP3 is accessed.
NC	4	r	**No Carrier** Set by HW to indicate no carrier. Clear this register by SW Read or after EP3 is accessed.

Field	Bits	Type	Description
LC	3	r	**Loss Carrier** Set by HW to indicate carrier loss. Clear this register by SW Read or after EP3 is accessed.
JTO	2	r	**Jabber Time Out** Set by HW to indicate jabber time out. Clear this register by SW Read or after EP3 is accessed.
Res	1:0	ro	**Reserved**

Transmit Status 2

TS2	Offset	Reset Value
Transmit Status 2	**$2C_H$**	**00_H**

7	6	5	4	3	2	1	0
TXFF	**TXFE**	Res		**TXPC**			
r	r	ro		r			

Field	Bits	Type	Description
TXFF	7	r	**TX Fifo Full** Set by HW to indicate tx fifo full. Clear this register by SW Read or after EP3 is accessed.
TXFE	6		**TX Fifo Empty** Set by HW to indicate tx fifo empty. Clear this register by SW Read or after EP3 is accessed.
Res	5:4	ro	**Reserved**
TXPC	3:0	r	**TX Packet Count** Set by HW to indicate Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted, this value will keep as 15. Clear this register by SW Read or after EP3 is accessed.

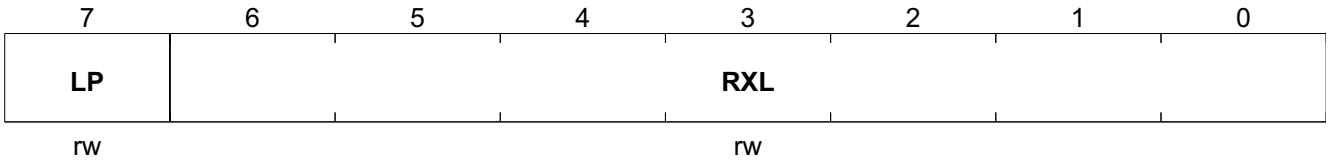
Receive Status

RS	Offset	Reset Value
Receive Status	$2D_H$	00_H

Field	Bits	Type	Description
Res	7:2	ro	**Reserved**
RXP	1	rw	**RX Pause** Set by HW to indicate a PAUSE frame is received. Clear this register by SW Read or after EP3 is accessed.
RXO	0	r	**RX Overflow** Set by HW to indicate external SRAM overflow. Clear this register by SW Read or after EP3 is accessed.

Receive Lost Packet Count High

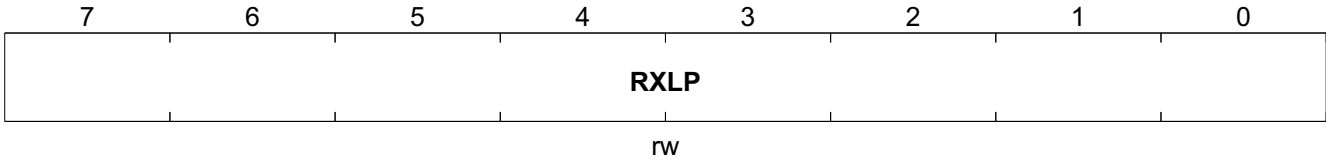
RLPCH	Offset	Reset Value
Receive Lost Packet Count High	$2E_H$	00_H



Field	Bits	Type	Description
LP	7	rw	**Received Packet Lost**
RXL	6:0		**RX Lost Packet Count** The [14:8] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed.

Receive Lost Packet Count Low

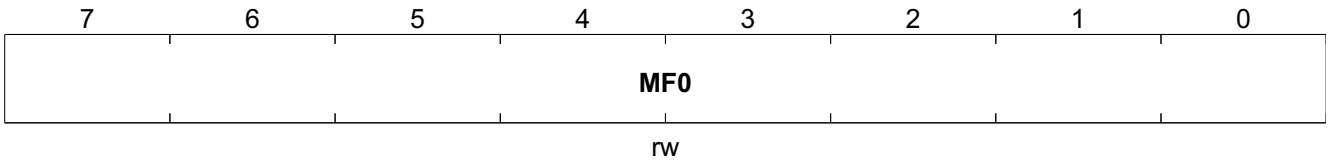
RLPCL	Offset	Reset Value
Receive Lost Packet Count Low	$2F_H$	00_H



Field	Bits	Type	Description
RXLP	7:0	rw	**RX Lost Packet** The [7:0] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed.

Wake-Up Frame 0 Mask 0

WUF0_M0	Offset	Reset Value
Wake-Up Frame 0 Mask 0	30_H	00_H



Field	Bits	Type	Description
MF0	7:0	rw	**The 128 Mask Bits for Frame 0**

Table 17 Wake-Up Frame 0 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF0_M1	Wake-Up Frame 0 Mask 1	31_H	
WUF0_M2	Wake-Up Frame 0 Mask 2	32_H	
WUF0_M3	Wake-Up Frame 0 Mask 3	33_H	
WUF0_M4	Wake-Up Frame 0 Mask 4	34_H	
WUF0_M5	Wake-Up Frame 0 Mask 5	35_H	
WUF0_M6	Wake-Up Frame 0 Mask 6	36_H	
WUF0_M7	Wake-Up Frame 0 Mask 7	37_H	
WUF0_M8	Wake-Up Frame 0 Mask 8	38_H	
WUF0_M9	Wake-Up Frame 0 Mask 9	39_H	

Table 17 Wake-Up Frame 0 Mask Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WUF0_M10	Wake-Up Frame 0 Mask 10	$3A_H$	
WUF0_M11	Wake-Up Frame 0 Mask 11	$3B_H$	
WUF0_M12	Wake-Up Frame 0 Mask 12	$3C_H$	
WUF0_M13	Wake-Up Frame 0 Mask 13	$3D_H$	
WUF0_M14	Wake-Up Frame 0 Mask 14	$3E_H$	
WUF0_M15	Wake-Up Frame 0 Mask 15	$3F_H$	

Wake-Up Frame 0 Offset

WUF0_O	Offset	Reset Value
Wake-Up Frame 0 Offset	**40_H**	**00_H**

7	6	5	4	3	2	1	0
OWUF0							
rw							

Field	Bits	Type	Description
OWUF0	7:0	rw	**Offset for Wake-up Frame 0**

Wake-Up Frame 0 CRC Low

WUF0_CRCL	Offset	Reset Value
Wake-Up Frame 0 CRC Low	**41_H**	**00_H**

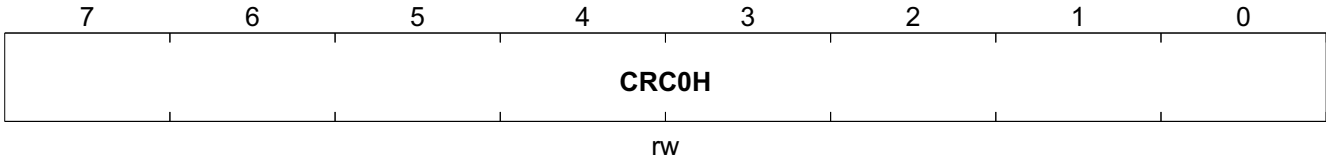
7	6	5	4	3	2	1	0
CRC0L							
rw							

Field	Bits	Type	Description
CRC0L	7:0	rw	**The Low Byte of CRC 16 Match for Frame 0**

Wake-Up Frame 0 CRC High

WUF0_CRCH **Offset** **Reset Value**

Wake-Up Frame 0 CRC High **42_H** **00_H**

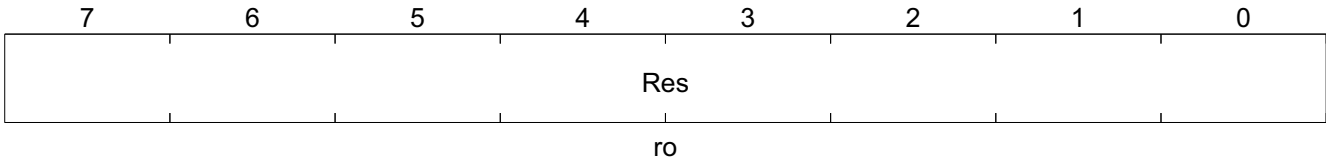


Field	Bits	Type	Description
CRC0H	7:0	rw	**The High Byte of CRC 16 Match for Frame 0**

Reserved 11

Res11 **Offset** **Reset Value**

Reserved 11 **43_H** **00_H**



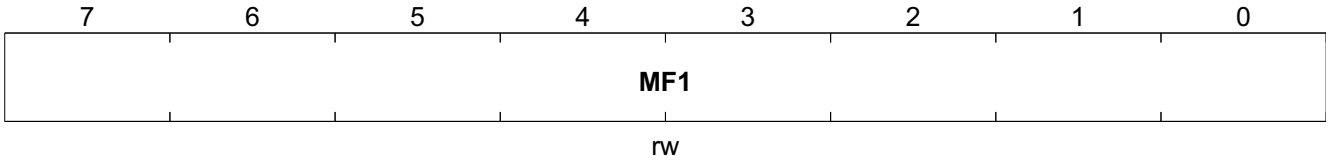
Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Table 18 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res12	Reserved12	44_H	
Res13	Reserved13	45_H	
Res14	Reserved14	46_H	
Res15	Reserved15	47_H	

Wake-Up Frame 1 Mask 0

WUF1_M0	Offset	Reset Value
Wake-Up Frame 1 Mask 0	48_H	00_H



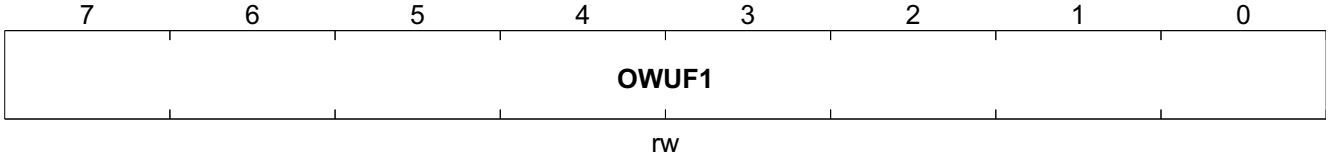
Field	Bits	Type	Description
MF1	7:0	rw	**The 128 Mask Bits for Frame 1**

Table 19 Wake-Up Frame 1 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF1_M1	Wake-Up Frame 1 Mask 1	49_H	
WUF1_M2	Wake-Up Frame 1 Mask 2	50_H	
WUF1_M3	Wake-Up Frame 1 Mask 3	51_H	
WUF1_M4	Wake-Up Frame 1 Mask 4	52_H	
WUF1_M5	Wake-Up Frame 1 Mask 5	53_H	
WUF1_M6	Wake-Up Frame 1 Mask 6	54_H	
WUF1_M7	Wake-Up Frame 1 Mask 7	55_H	
WUF1_M8	Wake-Up Frame 1 Mask 8	56_H	
WUF1_M9	Wake-Up Frame 1 Mask 9	57_H	

Wake-Up Frame 1 Offset

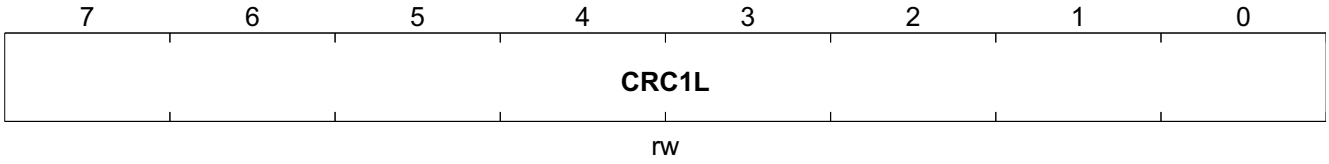
WUF1_O	Offset	Reset Value
Wake-Up Frame 1 Offset	58_H	00_H



Field	Bits	Type	Description
OWUF1	7:0	rw	**Offset for Wake-up Frame 1**

Wake-Up Frame 1 CRC Low

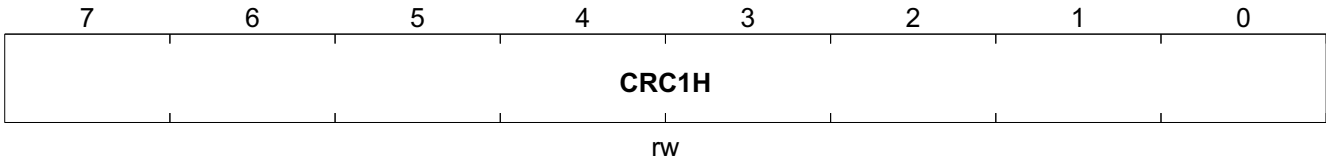
WUF1_CRCL	Offset	Reset Value
Wake-Up Frame 1 CRC Low	59_H	00_H



Field	Bits	Type	Description
CRC1L	7:0	rw	**The Low Byte of CRC 16 Match for Frame 1**

Wake-Up Frame 1 CRC High

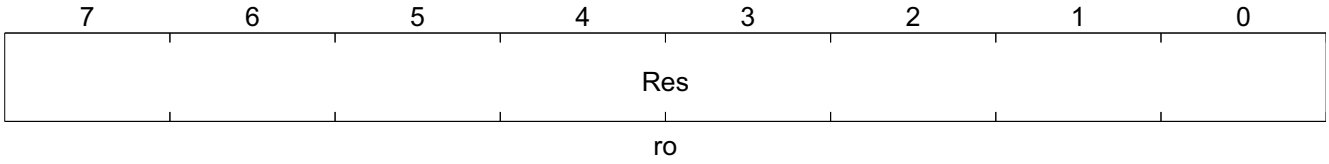
WUF1_CRCH	Offset	Reset Value
Wake-Up Frame 1 CRC High	$5A_H$	00_H



Field	Bits	Type	Description
CRC1H	7:0	rw	**The High Byte of CRC 16 Match for Frame 1**

Reserved 16

Res16	Offset	Reset Value
Reserved 16	$5B_H$	00_H



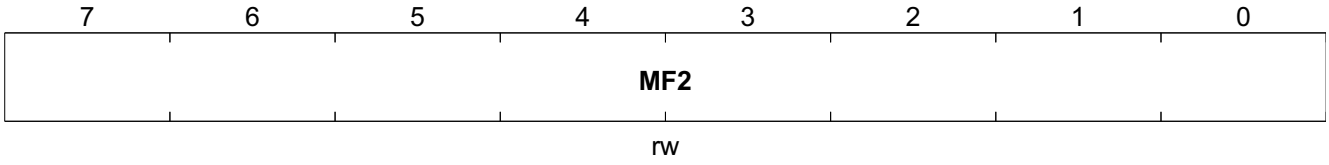
Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Table 20 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res17	Reserved 17	$5C_H$	
Res18	Reserved 18	$5D_H$	
Res19	Reserved 19	$5E_H$	
Res20	Reserved 20	$5F_H$	

Wake-Up Frame 2 Mask 0

WUF2_M0	Offset	Reset Value
Wake-Up Frame 2 Mask 0	60_H	00_H



Field	Bits	Type	Description
MF2	7:0	rw	**The 128 Mask Bits for Frame 2**

Table 21 Wake-Up Frame 2 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF2_M1	Wake-Up Frame 2 Mask 1	61_H	
WUF2_M2	Wake-Up Frame 2 Mask 2	62_H	

Table 21 Wake-Up Frame 2 Mask Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WUF2_M3	Wake-Up Frame 2 Mask 3	63_H	
WUF2_M4	Wake-Up Frame 2 Mask 4	64_H	
WUF2_M5	Wake-Up Frame 2 Mask 5	65_H	
WUF2_M6	Wake-Up Frame 2 Mask 6	66_H	
WUF2_M7	Wake-Up Frame 2 Mask 7	67_H	
WUF2_M8	Wake-Up Frame 2 Mask 8	68_H	
WUF2_M9	Wake-Up Frame 2 Mask 9	69_H	
WUF2_M10	Wake-Up Frame 2 Mask 10	$6A_H$	
WUF2_M11	Wake-Up Frame 2 Mask 11	$6B_H$	
WUF2_M12	Wake-Up Frame 2 Mask 12	$6C_H$	
WUF2_M13	Wake-Up Frame 2 Mask 13	$6D_H$	
WUF2_M14	Wake-Up Frame 2 Mask 14	$6E_H$	
WUF2_M15	Wake-Up Frame 2 Mask 15	$6F_H$	

Wake-Up Frame 2 Offset

WUF2_O	Offset	Reset Value
Wake-Up Frame 2 Offset	**70_H**	**00_H**

7	6	5	4	3	2	1	0
OWUF2							
rw							

Field	Bits	Type	Description
OWUF2	7:0	rw	**Offset for Wake-up Frame 2**

Wake-Up Frame 2 CRC Low

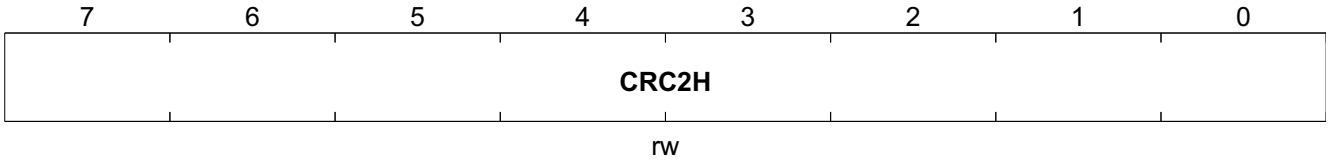
WUF2_CRCL	Offset	Reset Value
Wake-Up Frame 2 CRC Low	**71_H**	**00_H**

7	6	5	4	3	2	1	0
CRC2L							
rw							

Field	Bits	Type	Description
CRC2L	7:0	rw	**The Low Byte of CRC 16 Match for Frame 2**

Wake-Up Frame 2 CRC High

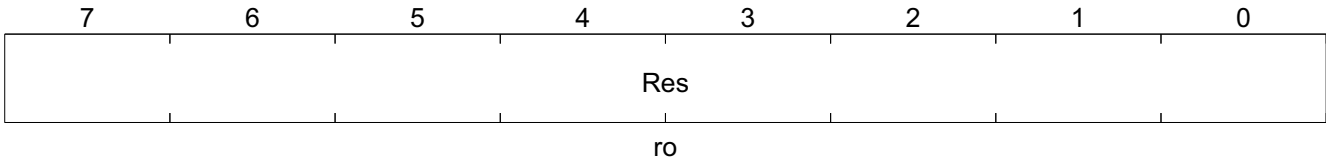
WUF2_CRCH	Offset	Reset Value
Wake-Up Frame 2 CRC High	72_H	00_H



Field	Bits	Type	Description
CRC2H	7:0	rw	**The High Byte of CRC 16 Match for Frame 2**

Reserved 21

Res21	Offset	Reset Value
Reserved 21	73_H	00_H



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Table 22 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res22	Reserved 22	74_H	
Res23	Reserved 23	75_H	
Res24	Reserved 24	76_H	
Res25	Reserved 25	77_H	

Wake-Up Control

WUC	Offset	Reset Value
Wake-Up Control	**78_H**	**04_H**

7	6	5	4	3	2	1	0
MPE	**LE**	**WF0E**	**WF1E**	**WF2E**	**C16T**	Res	
rw	rw	rw	rw	rw	rw	ro	

Field	Bits	Type	Description
MPE	7	rw	**Set by SW to Enable Magic Packet Wake-up Function**
LE	6		**Set by SW to Enable link Status Wake-up Function**
WF0E	5		**Set by SW to Enable Wakeup Frame 0 Wakeup Function**
WF1E	4		**Set by SW to Enable Wakeup Frame 1 Wakeup Function**
WF2E	3		**Set by SW to Enable Wakeup Frame 2 Wakeup Function**
C16T	2		**CRC16 Type** 0_B , CRC-16 initial contents = 0000_H 1_B , CRC-16 initial contents = $ffff_H$
Res	1:0	ro	**Reserved**

Reserved 26

Res26	Offset	Reset Value
Reserved 26	**79_H**	**00_H**

7	6	5	4	3	2	1	0
Res							
ro							

Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Wake-Up Status

WUS	Offset	Reset Value
Wake-Up Status	$7A_H$	00_H

7	6	5	4	3	2	1	0
RXMP	**LW**	**RXWF**	Res				**LS**
r	r	r	ro				r

Field	Bits	Type	Description
RXMP	7	r	**Set by HW when Receive a Magic Packet** Clear by SW read this register.
LW	6		**Set by HW when Link Status Change** Clear by SW read this register.
RXWF	5		**Set by HW when Receive a Wake-up Frame** Clear by SW read this register.
Res	4:1	ro	**Reserved**
LS	0	r	**Indicate the Current Link Status** 1 for link on, 0 for link off.

Internal PHY Control

IPHYC	Offset	Reset Value
Internal PHY Control	$7B_H$	00_H

7	6	5	4	3	2	1	0
Res						**PDP**	**PHYR**
ro						rw	rw

Field	Bits	Type	Description
Res	7:2	ro	**Reserved**
PDP	1	rw	**Power Down PHY** 0_B , Powers down internal 10/100 PHY 1_B , Enables internal 10/100 PHY
PHYR	0		**PHY Reset** The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0. 1_B , Reset internal PHY

GPIO 5:4

GPIO54 **Offset** **Reset Value**

GPIO 5:4 **$7C_H$** **00_H**

7	6	5	4	3	2	1	0
Res		**G5OE**	**G5OV**	**G5IV**	**G4OE**	**G4OV**	**G4IV**
ro		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
G5OE	5	rw	**GPIO5 Output Enable** 0_B , GPIO5 is used for input 1_B , GPIO5 is used for output
G5OV	4		**GPIO5 Output Value** When GPIO5 is used for output, this value is driven to GPIO5 pin. Set by SW.
G5IV	3	r	**GPIO5 Input Value** When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
G4OE	2	rw	**GPIO4 Output Enable** 0_B , GPIO4 is used for input 1_B , GPIO4 is used for output
G4OV	1		**GPIO4 Output Value** When GPIO4 is used for output, this value is driven to GPIO4 pin. Set by SW.
G4IV	0	r	**GPIO4 Input Value** When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

Reserved 27

Res27 **Offset** **Reset Value**

Reserved 27 **$7D_H$** **00_H**

7	6	5	4	3	2	1	0
Res							
ro							

Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

GPIO 1:0

GPIO10 **Offset** **Reset Value**

GPIO 1:0 **$7E_H$** **00_H**

7	6	5	4	3	2	1	0
Res		**G1OE**	**G1OV**	**G1IV**	**G0OE**	**G0OV**	**G0IV**
ro		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
G1OE	5	rw	**GPIO1 Output Enable** 1_D , GPIO1 is used for output 0_D , GPIO1 is used for input
G1OV	4		**GPIO1 Output Value** When GPIO1 is used for output, this value is driven to GPIO1 pin. Set by SW.
G1IV	3	r	**GPIO1 Input Value** When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.
G0OE	2	rw	**GPIO0 Output Enable** 0_B , GPIO0 is used for input 1_B , GPIO0 is used for output
G0OV	1		**GPIO0 Output Value** When GPIO0 is used for output, this value is driven to GPIO0 pin. Set by SW.
G0IV	0	r	**GPIO0 Input Value** When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.

GPIO 3:2

GPIO32 **Offset** **Reset Value**

GPIO 3:2 **$7F_H$** **00_H**

7	6	5	4	3	2	1	0
Res		G3OE	G3OV	G3IV	G2OE	G2OV	G2IV
ro		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
G3OE	5	rw	**GPIO3 Output Enable** 0_B , GPIO3 is used for input 1_B , GPIO3 is used for output
G3OV	4		**GPIO3 Output Value** When GPIO3 is used for output, this value is driven to GPIO3 pin. Set by SW.
G3IV	3	r	**GPIO3 Input Value** When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.
G2OE	2	rw	**GPIO2 Output Enable** 0_B , GPIO2 is used for input 1_B , GPIO2 is used for output
G2OV	1		**GPIO2 Output Value** When GPIO2 is used for output, this value is driven to GPIO2 pin. Set by SW.
G2IV	0	r	**GPIO2 Input Value** When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.

TEST Register

TR	Offset	Reset Value
TEST Register	**80_H**	**00_H**

7	6	5	4	3	2	1	0
Res			GS				UT
ro			rw				rw

Field	Bits	Type	Description
Res	7:5	ro	**Reserved**
GS	4:1	rw	**Internal Probing Signal Group Selection** group_sel
UT	0		**USB Test** 0_B , 6 test pins are used for USB transceiver 1_B , 6 test pins are used for internal signal probing

Test Mode

TM	Offset	Reset Value
Test Mode	81_H	02_H

7	6	5	4	3	2	1	0
Res			**TM**			**TTM**	Res
ro			rw			rw	ro

Field	Bits	Type	Description
Res	7:5	ro	**Reserved**
TM	4:2	rw	**This Value Could be Update from EEPROM Offset 0A 4:2** 000_B , Tri-state MII pins 001_B , Enables MAC's MII signals to external pins 010_B , Enables PHY's MII signals to external pins 011_B , Monitor mode MII
TTM	1		**This Value Could be Update from EEPROM Offset 0A 1** 0_B , External USB transceiver, GPIO[5:0] are used as external USB transceiver interface 1_B , Internal USB transceiver, GPIO[5:0] are used as GPIO pins
Res	0	ro	**Reserved**

4.2 Transceiver Registers

Table 23 Registers Address Space

Module	Base Address	End Address	Note
Transceiver Registers	0000 0000_H	0000 $001F_H$	

Table 24 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CTL	Control	00_H	67
STA	Status	01_H	68
PHYI1	PHY Identifier 1	02_H	69
PHYI2	PHY Identifier 2	03_H	70
ANA	Auto-Negotiation Advertisement	04_H	70
ANLPA	Auto-Negotiation Link Partner Ability	05_H	71
ANE	Auto Negotiation Expansion	06_H	72
ANNPT	Auto Negotiation Next Page Transmit	07_H	73
Res28	Reserved 28	08_H	75
Res29	Reserved 29	09_H	75
Res30	Reserved 30	$0A_H$	75
Res31	Reserved 31	$0B_H$	75
Res32	Reserved 32	$0C_H$	75
Res33	Reserved 33	$0D_H$	75
Res34	Reserved 34	$0E_H$	75
Res35	Reserved 35	$0F_H$	75
SPC	Specific	10_H	76
ICS	Interrupt Control/Status	11_H	77
DGN	Diagnostic	12_H	78
PWRLB	Power/Loopback	13_H	79
LPM	Loopback and Power Management	14_H	80
MCTL	Mode Control	15_H	80
Res36	Reserved 36	16_H	81
PLLL	PLL Lock	17_H	82
REC	Receive Error Counter	18_H	83
Res36	Reserved 36	19_H	75
Res37	Reserved 37	$1A_H$	75
Res38	Reserved 38	$1B_H$	75
Res39	Reserved 39	$1C_H$	75
Res40	Reserved 40	$1D_H$	75
Res41	Reserved 41	$1E_H$	75
Res42	Reserved 42	$1F_H$	75

The register is addressed wordwise.

Table 25 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 26 Registers Clock Domains

Clock Short Name	Description

4.2.1

Control

CTL	Offset	Reset Value
Control	00_H	1000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE	**LB**	**SS**	**ANE**	**PD**	**IS**	**RAN**	**DM**	**CT**	Res						
rwsc	rw	rw	rw	rw	rw	rwsc	rw	rw	rw						

Field	Bits	Type	Description
RE	15	rwsc	**Reset** This bit is self-clearing. 1_B , PHY reset
LB	14	rw	**Loopback** 0_B , Normal operation 1_B , Enables loopback mode. This will loopback TXD to RXD, thus it will ignore all the activity on the cable media.
SS	13		**Speed Select** This bit will be ignored if Auto Negotiation is enabled (0.12=1). 0_B , 10 Mbit/s 1_B , 100 Mbit/s
ANE	12		**Auto-Neg. Enable** 0_B , Disables auto-negotiate process 1_B , Enables auto-negotiate process (overrides 0.13 and 0.8)
PD	11		**Power Down** 0_B , Normal operation 1_B , Power down. ADM 8511 will shut off all blocks except for MDIO/MDC interface
IS	10		**Isolate** 0_B , Normal operation 1_B , Electrically isolate the PHY from MII. However, PHY is still able to response to MDC/MDIO
RAN	9	rwsc	**Restart Auto-Negotiation** 0_B , Normal operation 1_B , Restart Auto-Negotiation process

Field	Bits	Type	Description
DM	8	rw	**Dublex Mode** 0_B , Half duplex 1_B , Full duplex
CT	7		**Collision Test** 0_B , Disables COL test 1_B , Enables collision test, which issues the COL signal in response to the assertion of TX_EN signal
Res	6:0		**Reserved**

Status

STA	Offset	Reset Value
Status	01_H	7849_H

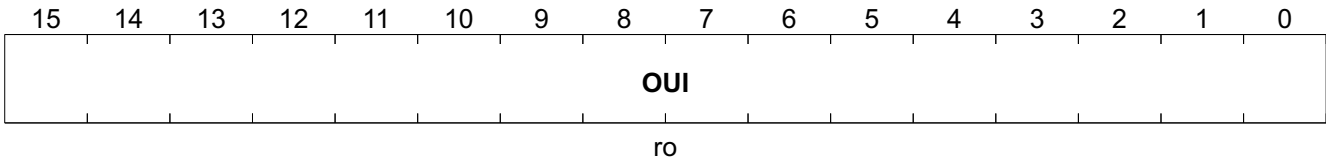
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100T4	**100FD**	**100HD**	**10FD**	**10HD**	Res					**ANC**	**RF**	**ANA**	**LS**	**JD**	**EC**
ro	ro	ro	ro	ro	ro					ro	ro/lh	ro	ro/ll	ro/lh	ro

Field	Bits	Type	Description
100T4	15	ro	**100Base-T4** Permanently tied to zero indicates no 100Base-T4 capability.
100FD	14		**100Base-TX Full Duplex** 0_B , No 100Base-TX full duplex ability 1_B , 100Base-TX with full duplex
100HD	13		**100Base-TX Half Duplex** 0_B , No TX half-duplex ability 1_B , 100Base-TX with half duplex
10FD	12		**10Base-T Full Duplex** 0_B , No 10BaseT full duplex ability 1_B , 10Base-T with full duplex
10HD	11		**10Base-T Half Duplex** 0_B , No 10Base-T half duplex ability 1_B , 10Base-T with half duplex
Res	10:6		**Reserved**
ANC	5		**Auto-Negotiate Complete** 0_B , Auto-negotiate process not completed 1_B , Auto-negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set
RF	4	ro/lh	**Remote Fault** This bit will remain set until it is cleared by reading register 1 via management interface. 0_B , No remote fault 1_B , Remote fault condition detected

Field	Bits	Type	Description
ANA	3	ro	**Auto-Negotiate Ability** 0_B , Unable to perform Auto-Negotiation function 1_B , Able to perform Auto-Negotiation function
LS	2	ro/ll	**Link Status** 0_B , Link is down 1_B , Link is established. This is Latched bit. Therefore, if ADM8511/X link failed, this bit will be cleared and remain “0” until register is read again via management interface
JD	1	ro/lh	**Jabber Detect** 0_B , No Jabber condition detected 1_B , Jabber condition detect
EC	0	ro	**Extended Capability** 1_B , Extended register capable. This bit is tied permanently to one

PHY Identifier 1

PHYI1	Offset	Reset Value
PHY Identifier 1	02_H	0022_H

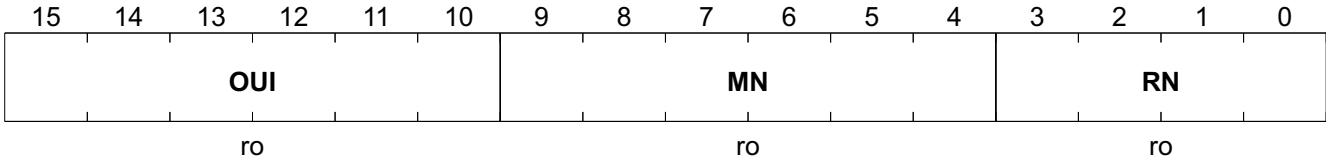


Field	Bits	Type	Description
OUI	15:0	ro	**Organizationally Unique Identifier** Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.

PHY Identifier 2

PHYI2 **Offset** **Reset Value**

PHY Identifier 2 **03_H** **5513_H**

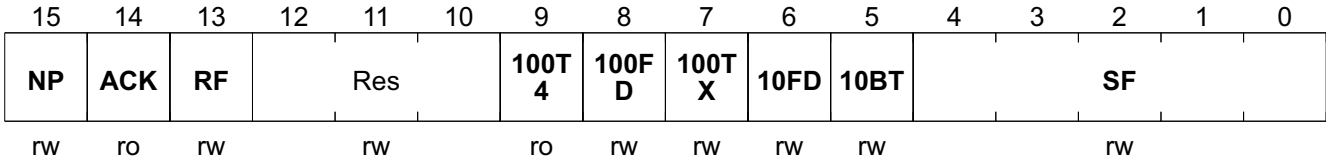


Field	Bits	Type	Description
OUI	15:10	ro	**Organizationally Unique Identifier** Assigned to the 19th through 24th bits of the OUI.
MN	9:4		**Model Number** Six bit manufacturer's model number.
RN	3:0		**Revision Number** Four bit manufacturer's revision number.

Auto-Negotiation Advertisement

ANA **Offset** **Reset Value**

Auto-Negotiation Advertisement **04_H** **$01E1_H$**

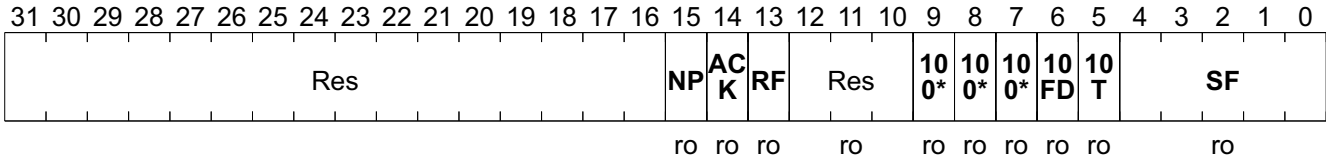


Field	Bits	Type	Description
NP	15	rw	**Next Page** 0_B , Next Page disabled 1_B , Next Page enabled
ACK	14	ro	**Acknowledge** This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.
RF	13	rw	**Remote Fault** 0_B , No remote fault detected 1_B , Advertises that this device has detected a Remote Fault
Res	12:10		**Reserved** For future technology.
100T4	9	ro	**100Base-T4** This bit ties to zero.

Field	Bits	Type	Description
100FD	8	rw	**100Base-TX Full Duplex** Default is set by Reg. 1.14. 0_B , 100Base-TX full duplex not supported by Local device 1_B , 100Base-TX full duplex supported by Local device
100TX	7		**100Base-TX** Default is set by Reg. 1.13. 0_B , 100Base-TX not supported by Local device 1_B , 100Base-TX supported by Local device
10FD	6		**10Base-T Full Duplex** Default is set by Reg. 1.12. 0_B , 10 Mbit/s full duplex not supported by Local device 1_B , 10 Mbit/s full duplex supported by Local device
10BT	5		**10Base-T** Default is set by Reg. 1.11. 0_B , 10 Mbit/s not supported by Local device 1_B , 10 Mbit/s supported by Local device
SF	4:0		**Selector Field** Protocol Selection [00001] = IEEE 802.3.

Auto-Negotiation Link Partner Ability

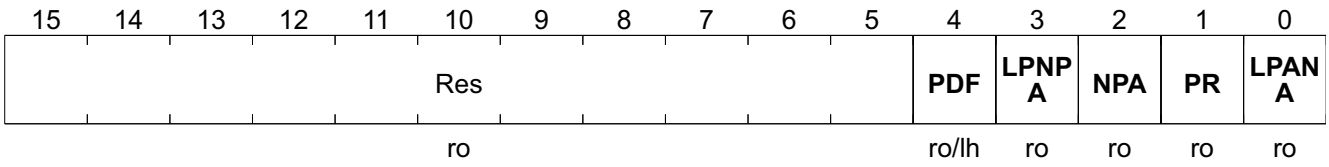
ANLPA	Offset	Reset Value
Auto-Negotiation Link Partner Ability	**05_H**	**0001_H**



Field	Bits	Type	Description
NP	15	ro	**Next Page** 0_B , Link partner does not desire Next Page transfer 1_B , Link partner desires Next Page transfer
ACK	14		**Acknowledge** 0_B , Not acknowledged by Link Partner 1_B , Link Partner acknowledges reception of FLP words
RF	13		**Remote Fault** 0_B , No remote fault detected by Link Partner 1_B , Remote Fault indicated by Link Partner
Res	12:10		**Reserved** For future technology.
100T4	9		**100Base-T4** 0_B , 100Base-T4 not supported by Link Partner 1_B , 100Base-T4 supported by Link Partner
100FD	8		**100Base-TX Full Duplex** 0_B , 100Base-TX full duplex not supported by Link Partner 1_B , 100Base-TX full duplex supported by Link Partner
100TX	7		**100Base-TX** 0_B , 100Base-TX not supported by Link Partner 1_B , 100Base-TX supported by Link Partner
10FD	6		**10Base-T Full Duplex** 0_B , 10 Mbit/s full duplex not supported by Link Partner 1_B , 10 Mbit/s full duplex supported by Link Partner
10T	5		**10Base-T** 0_B , 10 Mbit/s not supported by Link Partner 1_B , 10 Mbit/s supported by Link Partner
SF	4:0		**Selector Field** Protocol Selection [00001] = IEEE 802.3.

Auto Negotiation Expansion

ANE	Offset	Reset Value
Auto Negotiation Expansion	**06_H**	**0004_H**



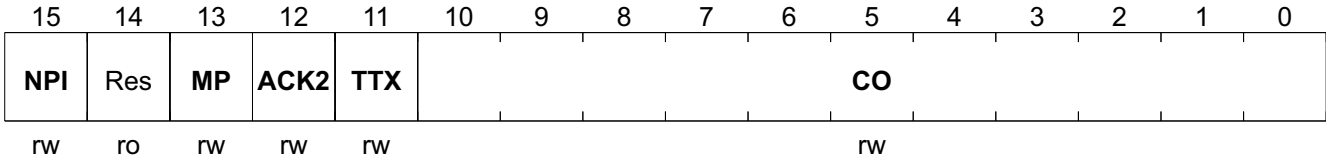
Field	Bits	Type	Description
Res	15:5	ro	**Reserved**

Field	Bits	Type	Description
PDF	4	ro/lh	**Parallel Detection Fault** 0_B , No fault detected by parallel detection logic 1_B , Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading this register and using the management interface
LPNPA	3	ro	**Link Partner Next Page Able** 0_B , Link partner does not support next page function 1_B , Link partner support next page function
NPA	2		**Next Page Able** Next page is supported, i.e., this bit is permanently tied to 1.
PR	1		**Page Received** It is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.
LPANA	0		**Link Partner Auto-Negotiation Able** 0_B , Link partner is not Auto-Negotiation capable 1_B , Link partner is Auto-Negotiation capable

Auto Negotiation Next Page Transmit Register

ANNPT **Offset** **Reset Value**

Auto Negotiation Next Page Transmit **07_H** **2001_H**

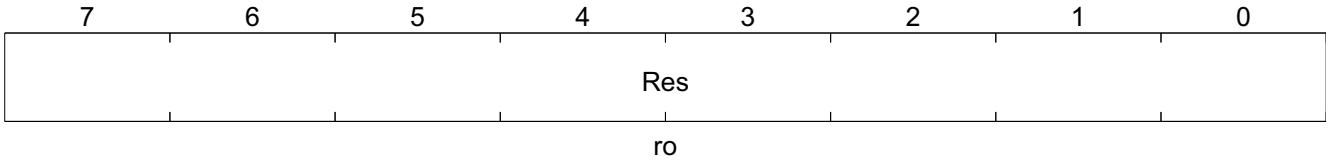


Field	Bits	Type	Description
NPI	15	rw	**Next Page Indication** 0_B , No other Next Page Transfer desired 1_B , Another Next Page desired
Res	14	ro	**Reserved**

Field	Bits	Type	Description
MP	13	rw	**Message Page** 0_B , Un-formatted page 1_B , Message page
ACK2	12		**Acknowledge 2** 0_B , Cannot comply with message 1_B , Will comply with message
TTX	11		**Toggle** 0_B , Previous value of transmitted link code word equals to 1 1_B , Previous value of transmitted link code word equals to 0
CO	10:0		**Code** Message/Un-formatted Code Field.

Reserved 28

Res28	Offset	Reset Value
Reserved 28	**08_H**	**$xxxx_H$**



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Table 27 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res29	Reserved 29	09_H	
Res30	Reserved 30	$0A_H$	
Res31	Reserved 31	$0B_H$	
Res32	Reserved 32	$0C_H$	
Res33	Reserved 33	$0D_H$	
Res34	Reserved 34	$0E_H$	
Res35	Reserved 35	$0F_H$	
Res36	Reserved 36	19_H	
Res37	Reserved 37	$1A_H$	
Res38	Reserved 38	$1B_H$	
Res39	Reserved 39	$1C_H$	
Res40	Reserved 40	$1D_H$	
Res41	Reserved 41	$1E_H$	
Res42	Reserved 42	$1F_H$	

Specific

SPC **Offset** **Reset Value**
Specific **10_H** **0540_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	**IL**	Res		**STI**	**10LB**	Res				**APD**	**RP**	Res			**RCC**
rw	rw	rw		rw	rw	ro				rw	rw	ro			rw

Field	Bits	Type	Description
RP	15	rw	**Repeater** 1_B , Repeater mode, full-duplex will be inactive, and CRS only responses to receive activity. SQE test function is also disabled
IL	14		INTR_LEVL INTR pin will be active high if this register bit is set to 1. INTR pin will be active low if this register bit is set to 0.
Res	13:12		**Reserved**
STI	11		**SQE Test Inhibit** 0_B , Enables 10BaseT SQE testing, which will generate a COL pulse following the completion of a packet transmission 1_B , Disable 10BaseT SQE testing
10LB	10		**10BaseT Loop Back** 0_B , Disables normal loopback in 10BaseT mode 1_B , Enables normal loopback in 10BaseT mode
Res	9:6	ro	**Reserved**
APD	5	rw	**Auto Polarity Disable** 0_B , Enables auto polarity detection / correction 1_B , Disables auto polarity detection / correction
RP	4		**Reverse Polarity** If Reg. 16.5 is set to 0, and Reverse polarity is detected on the media, this bit will get set to 1. If Reg. 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter. *Note: The reverse polarity is detected either through 8 inverted NLP or through a burst of inverted FLP*
Res	3:1	ro	**Reserved**
RCC	0	rw	**Receive Clock Control** Write a one this bit will shut off RX_CLK when incoming data is not present. RX_CLK will resume active 1 clock cycle prior to RX_DV goes high, and shut off 64 clock cycles after RX_DV goes low. However, in loopback, writing this bit does not affect RX_CLK. Receive clock will be active all the time.

Interrupt Control/Status

ICS	Offset	Reset Value
Interrupt Control/Status	11_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JIE	REI	PRI	PFI	LAI	LNOI	RFI	ANCIE	JIN	REI	PRIN	PFIN	LAIN	LNOIN	RFIN	ANCIN
rw	rw	rw	rw	rw	rw	rw	rw	rc	rc	rc	rc	rc	rc	rc	rc

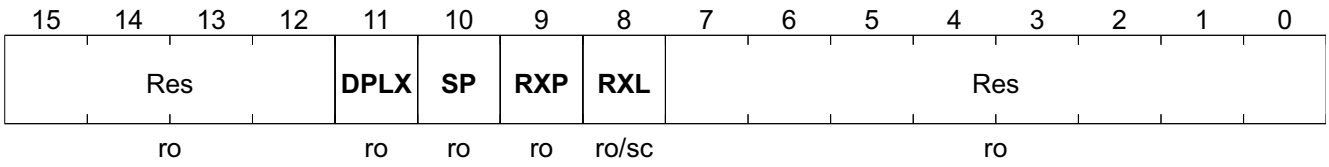
Field	Bits	Type	Description
JIE	15	rw	**Jabber Interrupt Enable** Jabber_IE
REI	14		**Receive Error Interrupt Enable** Rx_Er_IE
PRI	13		**Page Received Interrupt Enable** Page_Rx_IE
PFI	12	rw	**Parallel Detection Fault Interrupt Enable** PD_Fault_IE
LAI	11		**Link Partner Acknowledge Interrupt Enable** LP_Ack_IE
LNOI	10		**Link Status Not OK Interrupt Enable** Link_Not_OK_IE
RFI	9		**Remote Fault Interrupt Enable** R_Fault_IE
ANCIE	8		**Auto-Negotiation Complete Interrupt Enable** ANeg_Comp_IE

Field	Bits	Type	Description
JIN	7	rc	**This Bit is Set when a Jabber Event is Detected** Jabber_Int
REI	6		**This Bit is Set when RX_ER Transitions High** Rx_Er_Int
PRIN	5		**This Bit is Set when a New Page is Received from Link Partner During Auto-Neg.** Page_Rx_Int
PFIN	4		**This Bit is Set when Parallel Detect Fault is Detected** PD_Fault_Int
LAIN	3		**This Bit is Set when the FLP with Acknowledge Bit Set is Received** LP_Ack_Int
LNOIN	2		**This Bit is Set when Link Status Switches from OK Status to Non-OK Status (Fail or Ready)** Link_Not_OK Int
RFIN	1		**This Bit is Set when Remote Fault is Detected** R_Fault_Int
ANCIN	0		**This Bit is Set when Auto-Neg is Complete** A_Neg_Comp Int

Note: See Interrupt Table for bit Assignments

Diagnostic

DGN	Offset	Reset Value
Diagnostic	**12_H**	**0000_H**



Field	Bits	Type	Description
Res	15:12	ro	**Reserved**
DPLX	11		**Duplex** This bit indicates the result of the Auto-Neg for duplex arbitration.
SP	10		**Speed** This bit indicates the result of the Auto-Neg for data speed arbitration.
RXP	9		**RX_PASS** In 10BT mode, this bit indicates that Manchester data has been detected. In 100BT mode, it indicates valid signal has been received but not necessarily locked on to.

Field	Bits	Type	Description
RXL	8	ro/sc	**RX_LOCK** Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10Base-T or 100Base-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read.
Res	7:0	ro	**Reserved**

Power/Loopback

PWRLB **Offset** **Reset Value**

Power/Loopback **13_H** **0020_H**

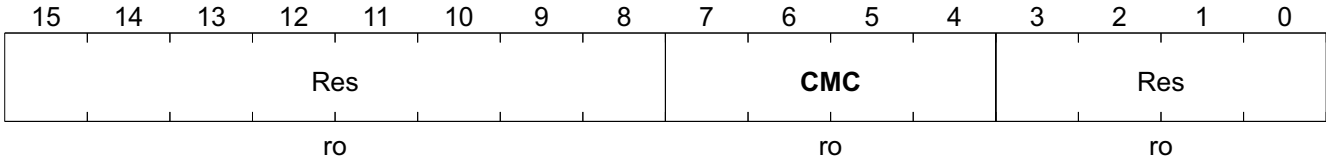
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res								**TTRS**	**LPM**	**TLB**	**DLP**	**LPBK**	**NLIT**	**RT**
	ro								rw	rw	rw	rw	rw	rw	r

Field	Bits	Type	Description
Res	14:7	ro	**Reserved**
TTRS	6	rw	**Transmit Transformer Ratio Selection** TP125 0_B , 1:1 1_B , 1.25:1
LPM	5		**Low Power Mode** 0_B , Disables advanced power saving mode 1_B , Enables advanced power saving mode
TLB	4		**Test Loopback** 1_B , Enables test loopback. Data will be transmitted from MII interface to clock recovery and loopback to MII received data
DLP	3		**Digital Loopback** 0_B , Normal operation 1_B , Enables loopback
LPBK	2		LP_LPBK 0_B , Normal operation 1_B , Enables link pulse loopback
NLIT	1		**NLP Link Integrity Test** 0_B , Sending FLP in Auto-Neg test mode 1_B , In Auto-Neg test mode, send NLP instead of FLP in order to test NLP receive integrity
RT	0	r	**Reduce Timer** 0_B , Normal operation 1_B , Reduce time constant for Auto-Negotiation timer

Loopback and Power Management

LPM **Offset** **Reset Value**

Loopback and Power Management **14_H** **$xxFx_H$**

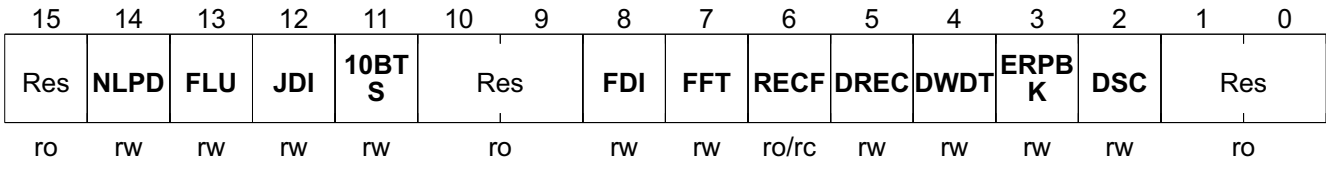


Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
CMC	7:4		**Cable Measurement Capability** These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute.
Res	3:0		**Reserved**

Mode Control

MCTL **Offset** **Reset Value**

Mode Control **15_H** **0304_H**



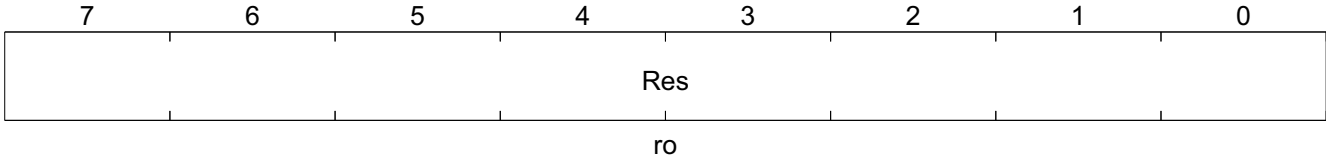
Field	Bits	Type	Description
Res	15	ro	**Reserved**

Field	Bits	Type	Description
NLPD	14	rw	**NLP Disable** 0_B , Normal Operation 1_B , Force 10B-T link up without checking NLP
FLU	13		Force_link_up 1_B , Force link up, auto negotiation must be disabled at this time
JDI	12		**Jabber Disable** 0_B , Enables Jabber function in PHY 1_B , Disables Jabber function in PHY
10BTS	11		10BT_Sel 0_B , Normal operation 1_B , Enables 7-wire interface for 10Base-T operation. This bit is useful only when the chip is not in PCS bypass mode
Res	10:9	ro	**Reserved**
FDI	8	rw	FEF_Disable 0_B , Disables far-end-fault 1_B , Enables far-end-fault generation and detection function
FFT	7		**Force FEF Transmit** This bit is set to force to transmit Far End Fault (FEF) pattern.
RECF	6	ro/rc	Rx_Er_Cnt Full When Receive Error Counter is full, this bit will get set to one.
DREC	5	rw	Disable Rx_Er_Cnt 0_B , Enables Receive Error Counter 1_B , Disables Receive Error Counter
DWDT	4		Dis_WDT 0_B , Enables watchdog timer 1_B , Disables the watchdog timer in the decipher
ERPBK	3		En_RPBK 0_B , Disables remote loopback 1_B , Enables remote loopback
DSC	2		Dis_Scrm When FX mode is selected, this bit will be forced to one 0_B , Disables data scrambling 1_B , Enables data scrambling
Res	1:0	ro	**Reserved**

Reserved 36

Res36 **Offset** **Reset Value**

Reserved 36 **16_H** **$xxxx_H$**

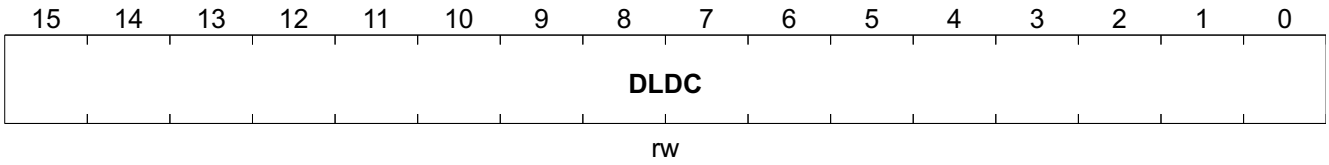


Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

PLL Lock

PLLL **Offset** **Reset Value**

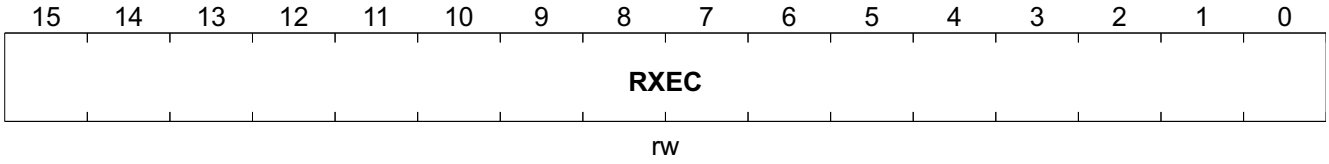
PLL Lock **17_H** **0000_H**



Field	Bits	Type	Description
DLDC	15:0	rw	**DLOCK Drop Counter** Count PLL lock drop events.

Receive Error Counter

REC	Offset	Reset Value
Receive Error Counter	18_H	0000_H



Field	Bits	Type	Description
RXEC	15:0	rw	**RX Error Counter** Count receive error events.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 28 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	–	–	4.6	V	–
DC Input Voltage	V_{IN}	–	–	6	V	–
DC Output Voltage	V_{OUT}	–	–	4.6	V	–
Power Consumption	I_{PC}	–	–	64	mA	Idle state
		–	–	120	mA	10M Full Duplex Mode
		–	–	150	mA	100M Full Duplex Mode
Storage Temperature	T_S	-65	–	150	°C	–
Ambient Temperature	T_A	-40	–	125	°C	–
ESD robustness	V_{ESD}	–	–	2000	V	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 29 Operating Condition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	3.0	–	3.6	V	–
Supply Current	I_{DD}	–	–	150	mA	–

5.2 DC Characteristics

Table 30 USB Interface DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Differential Input Sensitivity	V_{DI}	0.2	–	–	V	–
Differential Common Mode Range	V_{CM}	0.8	–	2.5	V	–
Output Low Voltage	V_{OL}	0.0	–	0.3	V	–

Table 30 USB Interface DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High Voltage	V_{OH}	2.8	–	3.6	V	–
Output Signal Crossover Voltage	V_{CRS}	1.3	–	2.0	V	–

Recommended Operating Conditions.

Table 31 EEPROM Interface DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	±1	–	1000	nA	V_{IN} = 3.3 V or 0 V
Output High Voltage	V_{CH}	2.4	–	–	V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.66	pF	–

Table 32 Home PNA Interface DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	±1	–	1000	nA	V_{IN} = 3.3 V or 0 V
Output High Voltage	V_{OH}	2.4	–		V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.63	pF	–

Table 33 GPIO Interface DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	±1	–	1000	nA	V_{IN} = 3.3 V or 0 V
Output High Voltage	V_{OH}	2.4	–	–	V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.64	pF	–

5.3 Reset Timing

ADM8511/X can be reset either by hardware, software or USB reset.

- A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 100 ms to ensure the external 48 MHz crystal is in stable and correct frequency. All registers will be reset to default values.

- A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01_H). This software reset will reset all registers to default values.
- When ADM8511/X sees an SE0 on USB bus for more than 2.5 µs. This USB reset will reset all registers to default values.

5.4 USB Interface Timing

Table 34 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time	T_{FR}	4	–	20	ns	C_L = 50 pF
Fall time	T_{FF}	4	–	20	ns	C_L = 50 pF
Rise and fall time matching	T_{FRFF}	90	–	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Table 35 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Clock Frequency	t_{EESK}	0	–	1	MHz	–
EECS Setup Time to EESK	T_{EECSS}	0.2	–	–	µs	–
EECS Hold Time from EESK	T_{EECSH}	0	–	–	ns	–
EEDO Hold Time from EESK	T_{EEDOH}	70	–	–	ns	–
EEDO Output Delay to “1” or “0”	T_{EEDOP}	–	–	2	µs	–
EEDI Setup Time to EESK	t_{EEDIS}	0.4	–	–	µs	–
EEDI Hold Time from EESK	t_{EEDIH}	0.4	–	–	µs	–

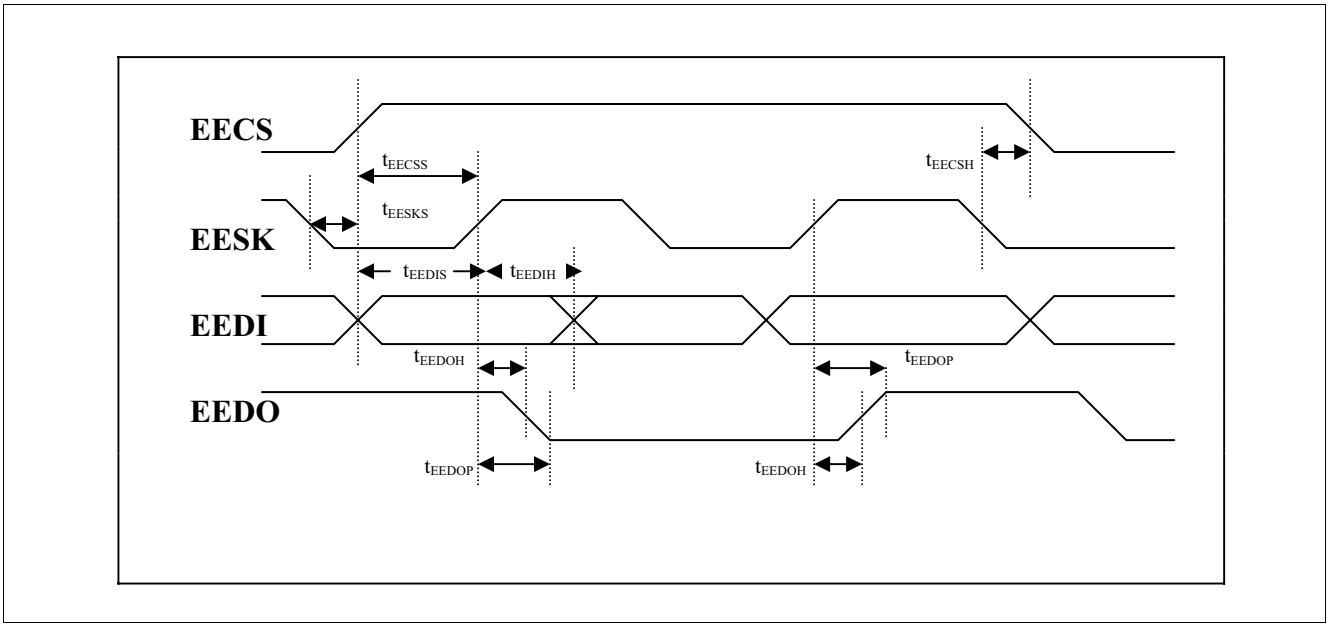


Figure 3 EEPROM Interface Timings

5.5 Home PNA Interface Timing

Table 36 Home PNA Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HPN_TXCLK during MAC preamble and delimiter		100e-9	–	100e-6	s	–
HPN_TXCLK during Ethernet packet		100e-9	–	10e-6	s	–
HPN_RXCLK during MAC preamble and delimiter		100e-9	–	100e-6	s	–
HPN_RXCLK during Ethernet packet		100e-9	–	10e-6	s	–
HPN_TXCLK and HPN_RXCLK during 96-bit inter-frame gap		233.334	–	233.334	ns	–
HPN_TXCLK and HPN_RXCLK during idle		583.335	–	583.335	ns	–

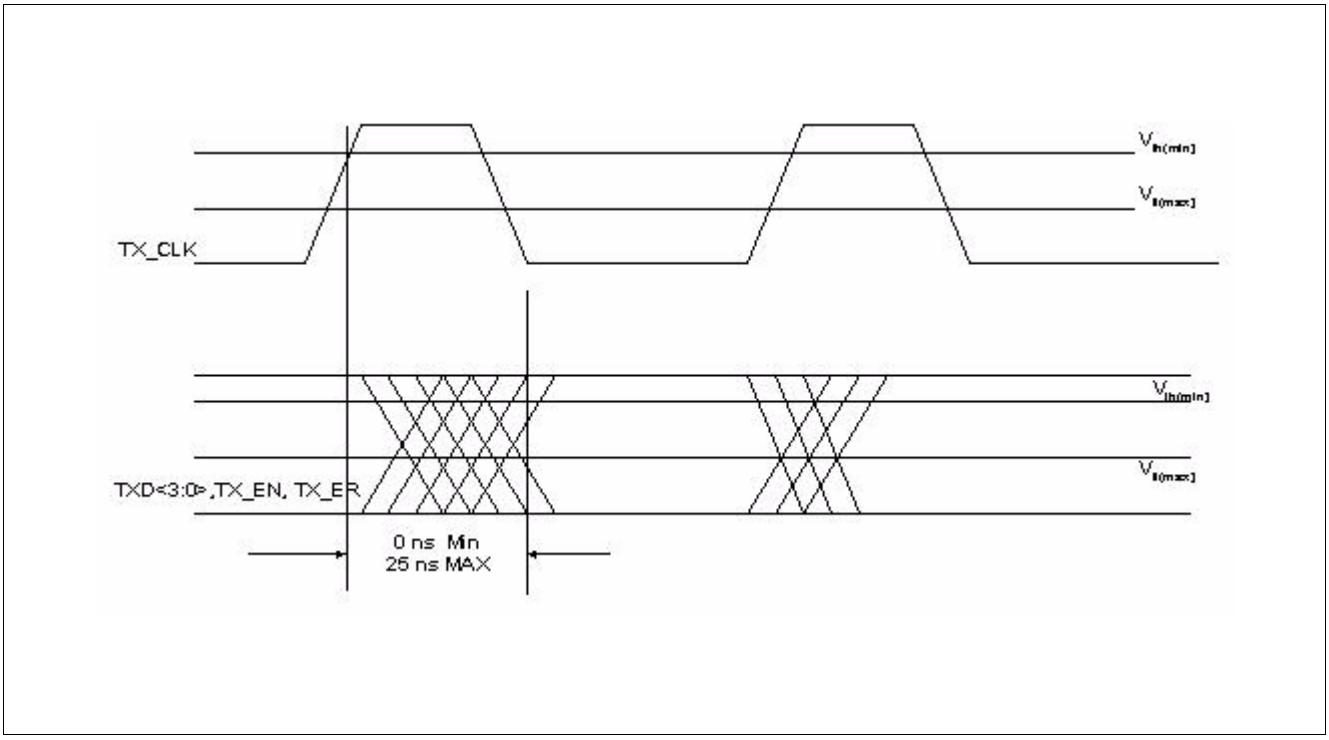


Figure 4 Transmit Signal Timing Relationships at the MII

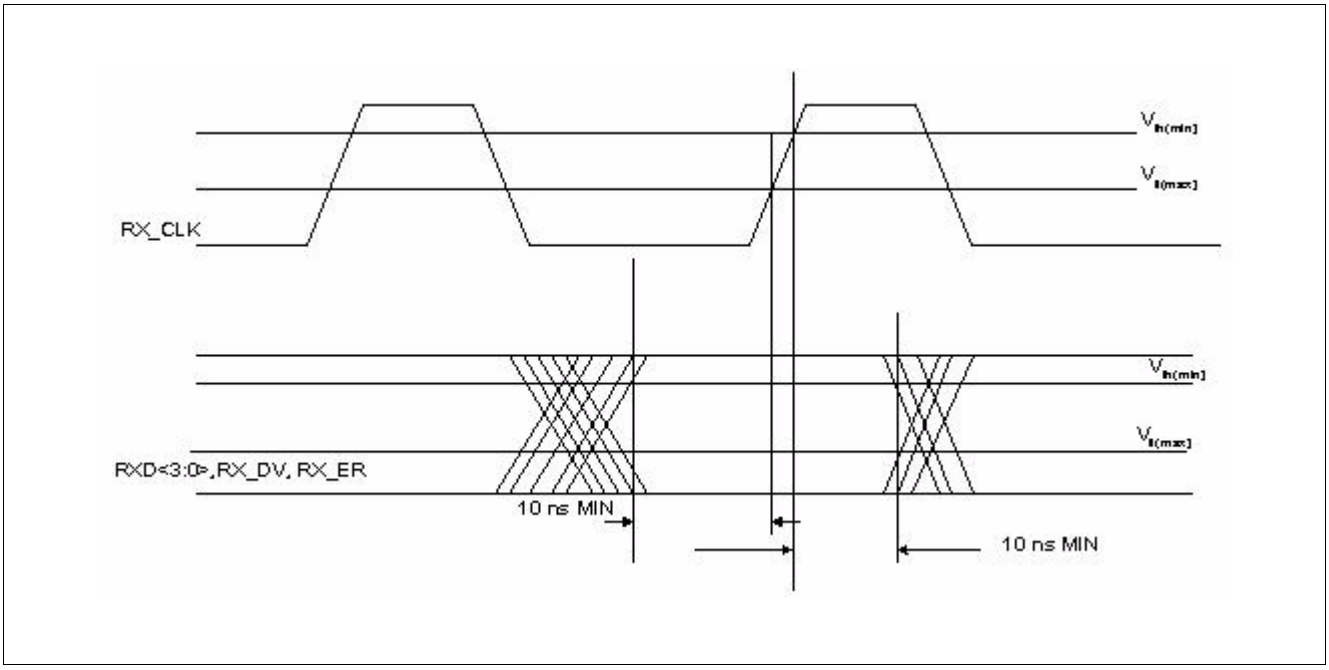


Figure 5 Receive Signal Timing Relations at the MII

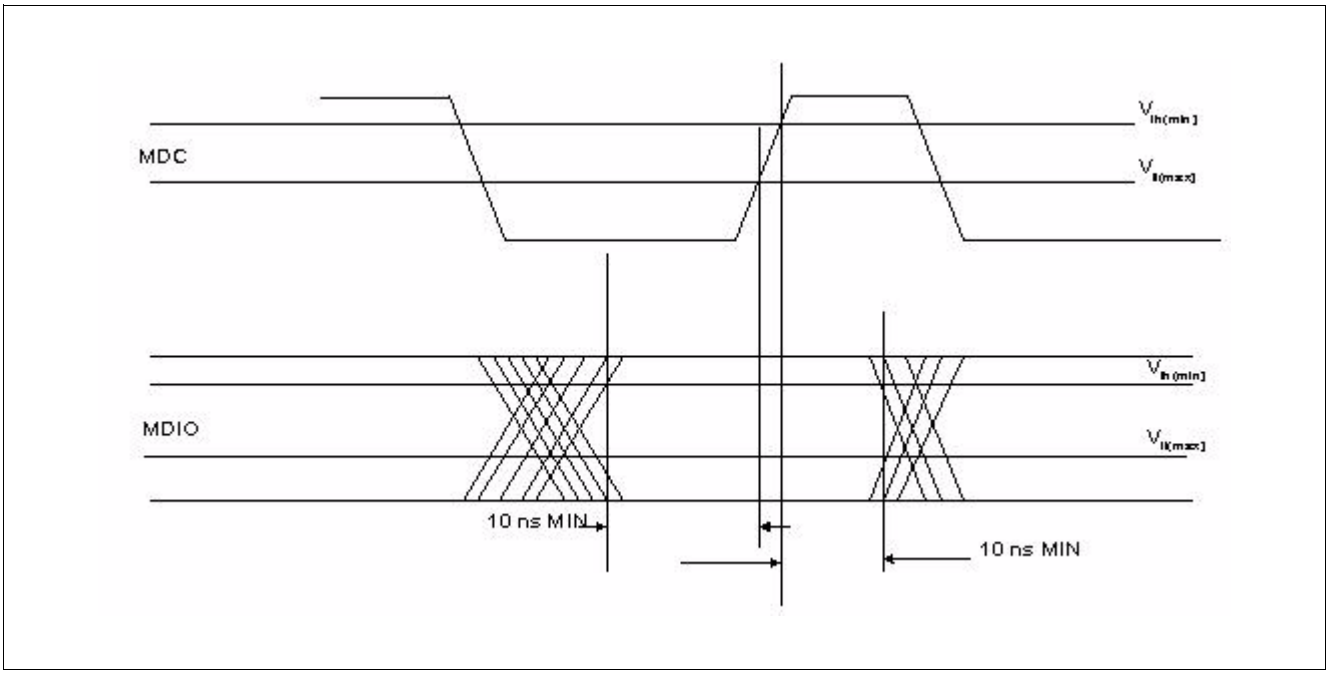


Figure 6 MDIO Sourced by STA

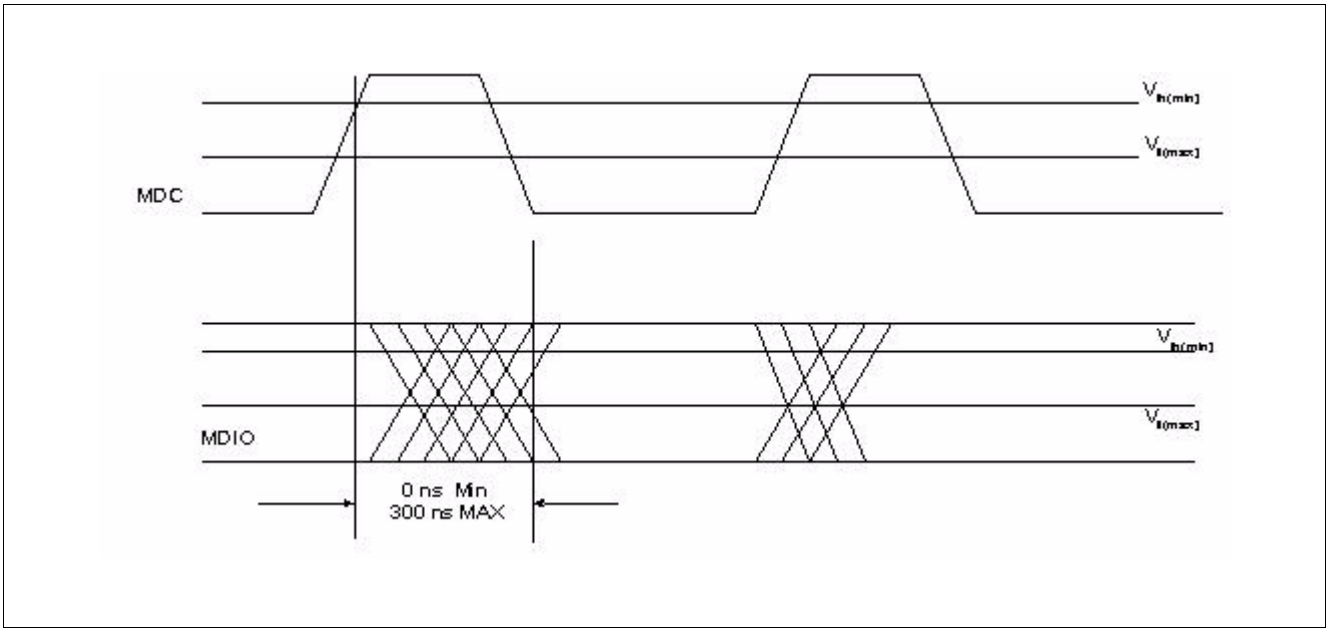


Figure 7 MDIO Sourced by PHY

6 Packaging

Package Outline of ADM8511/X, P-LQFP-100

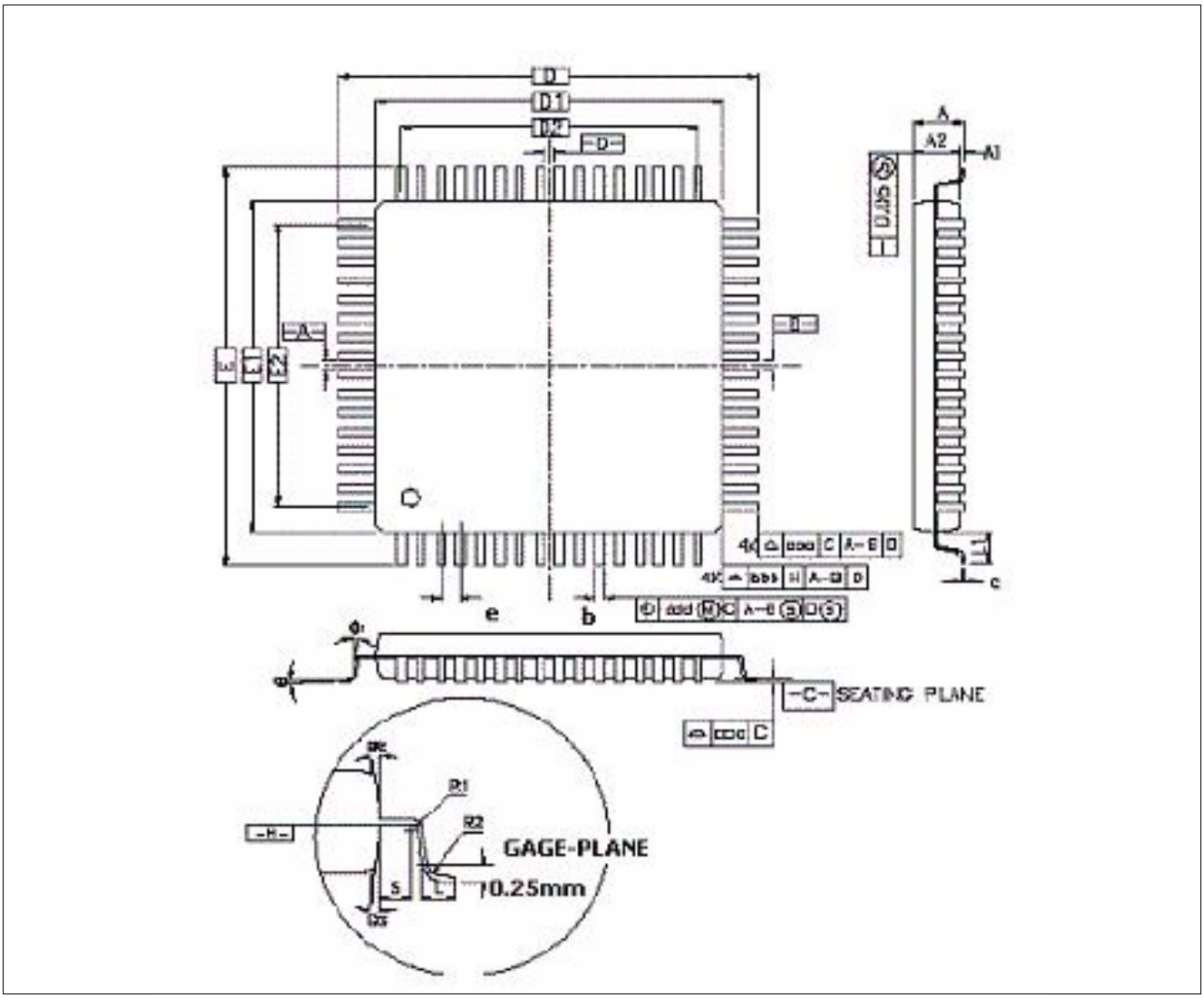


Figure 8 **P-LQFP-100-1** (Plastic Low Profile Quad Flat Package)

Note: Dimensions in mm

Table 37 Dimensions for 100 Pin LQFP Package

Symbol	Millimeter (mm)			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.005	0.057
D		16.00 BSC.			0.630 BSC.	
D_1		14.00 BSC			0.551 BSC.	
E		16.00 BSC			0.630 BSC.	
E_1		14.00 BSC			0.551 BSC.	
R_2	0.08	–	0.20	0.003	–	0.008
R_1	0.08	–	–	0.003	–	–
Θ	0°	3.5°	7°	0°	3.5°	7°
$Θ_1$	0°	–	–	0°	–	–
$Θ_2$	11°	12°	13°	11°	12°	13°
$Θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 Ref.			0.039 Ref.	
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e		0.50 BSC.			0.020 BSC.	
D_2		12.00			0.472	
E_2		12.00			0.472	
Tolerance of Form and Position						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.08			0.003	

Note:

1. *Dimensions D_1 and E_1 do not include mold protrusion. Allowable protrusion is 0.25 mm per. Side D_1 and E_1 are Maximum plastic body size dimensions including mold mismatch.*
2. *Dimensions b does not include dambar protrusion stall not cause the lead width to exceed the maximum b dimensions by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Maximum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*

7 APPENDIX 1 - Layout Guide

7.1 Placement

1. On USB side, Place PegasusII and USB connector as close as possible.
2. On Ethernet side,place PegasusII, transformer and RJ45 as close as possible.
3. The crystal or OSC device should be close to PegasusII and away from the following items:
   a) Any analog signal
   b) PCB edge
   c) Any other high frequency components and their associated traces.
4. Place the filtering capacitor as close as possible at the power pin of ADM 8511 (Pegasus II) and its trace is short and wide.

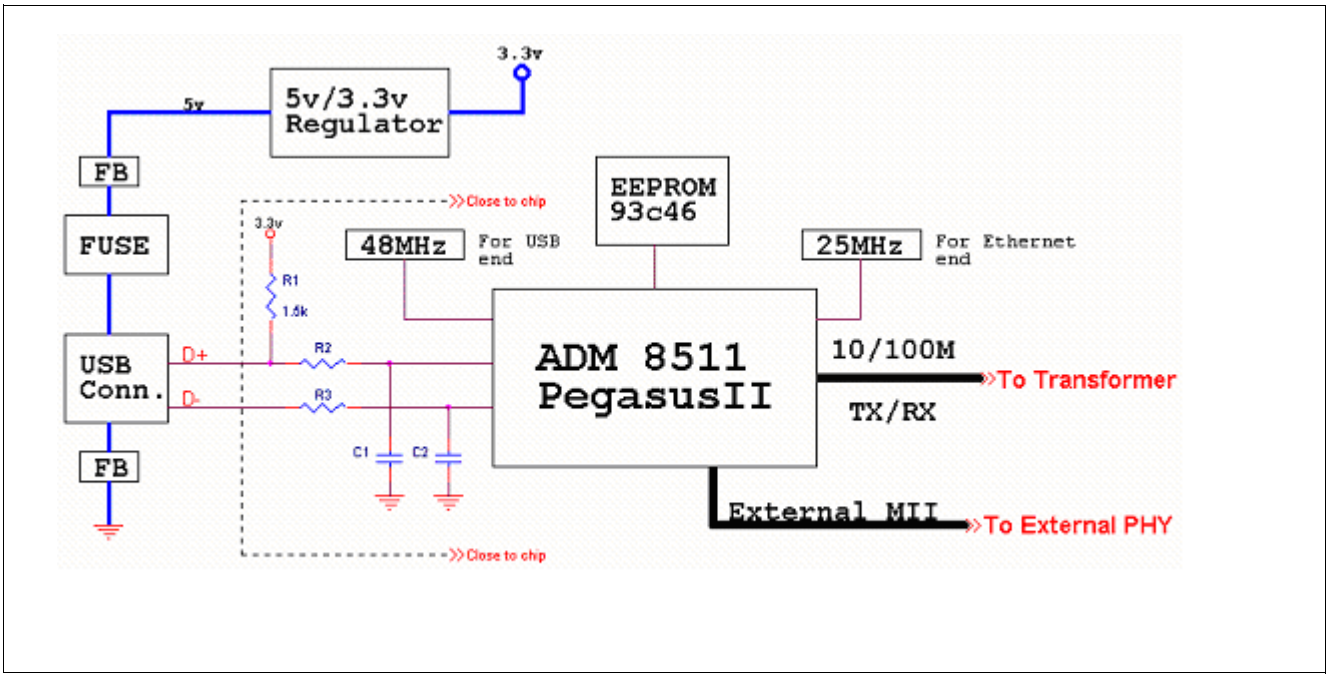


Figure 9 Correct placement

7.2 Trace routing

- Keep USB differential pair data signal D+ and D-:
  - Trace width should be as wide as possible.
  - Make D+ and D- traces route at the same signal plane and doesn't pass through other plane.
  - Inhibit crossover on D+ and D-
  - The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be close to ADM8511/X.
  - D+ and D- Signal trace length should be equal and as short as possible
- Arrangement Tx and Rx trace
  - Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree; suggested.

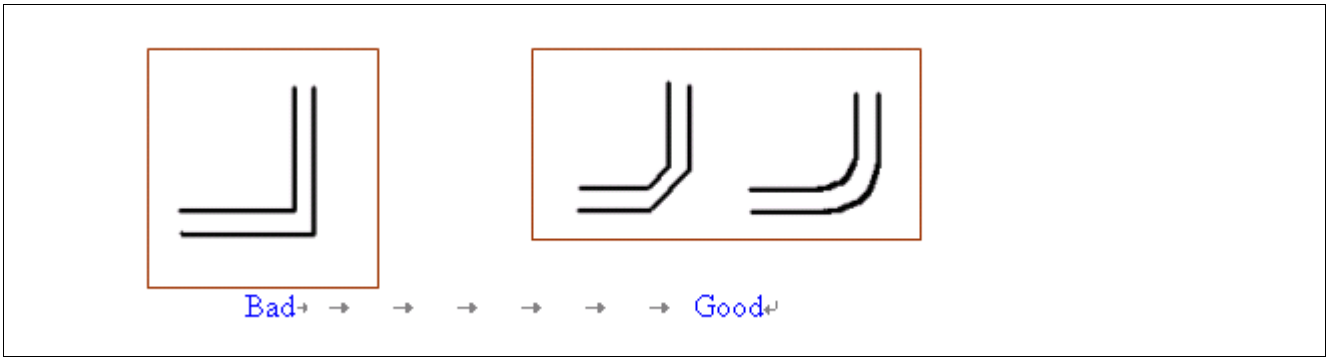


Figure 10 Trace routing

- Trace width must be wide and should be wider than 8 miles.
  - Signal trace length between Tx+/- differential pairs should be cross and have equal length.The total length should be no longer than 2 cm. The same requirement also apply to Rx+/-.
  - Make Tx and Rx trace route at the same signal plane and doesn't pass through other plane.
  - Every differential pairs as cross as possible, but no less than 8 miles and space should be almost equal
  - Keep space large between Tx and Rx differential pairs, even separated ground planes underneath Tx and Rx signal pairs
  - Away from clock and power traces.
  - If Tx routed trace must cross, the trace can be swapped between chip and transformer, and transformer to RJ45, too.

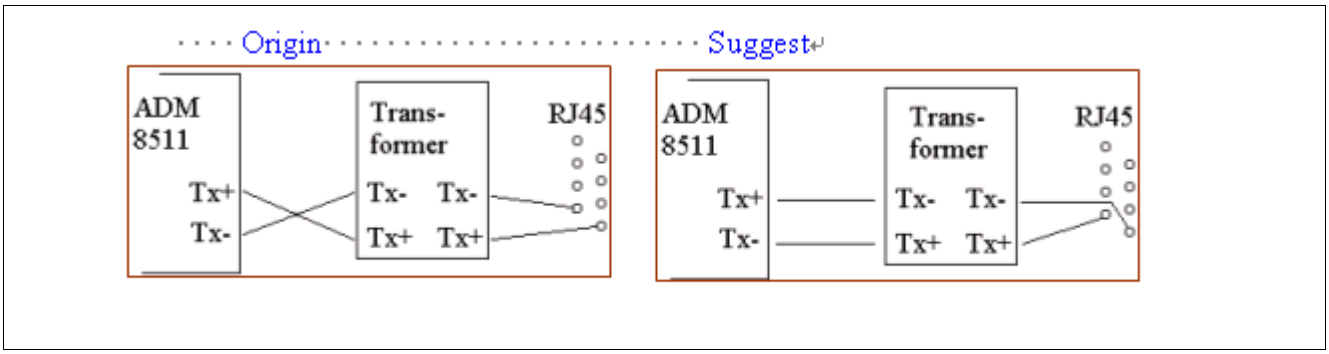


Figure 11 Crossed Tx routed trace

- Digital signal should be away from analog signal and power traces. If this can't be avoided, analog and VCC should cross over 90 degree at other plane.
- Vcc trace should short and prefer to route in this plane format, special for GND.

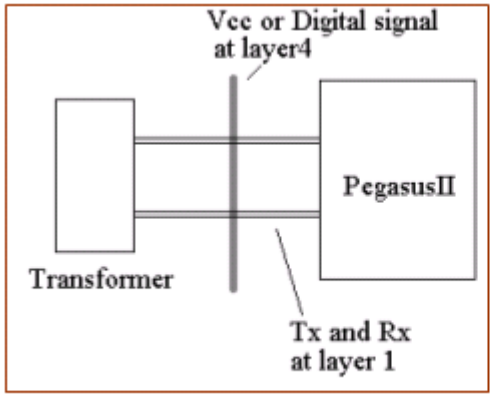


Figure 12 Vcc trace

7.3 Power and Ground

- Every power pin should have 0.1uF SMD capacitors placed with it. To be effective, the capacitors should be placed as close as possible at the pin.
- The chassis ground plane connected to the USB B type and network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in FCC failure.
- Right angle is recommend when partition Vcc as well as GND planes.
- Avoid power and ground planes placing directly under the transformer.See **Figure 13**.

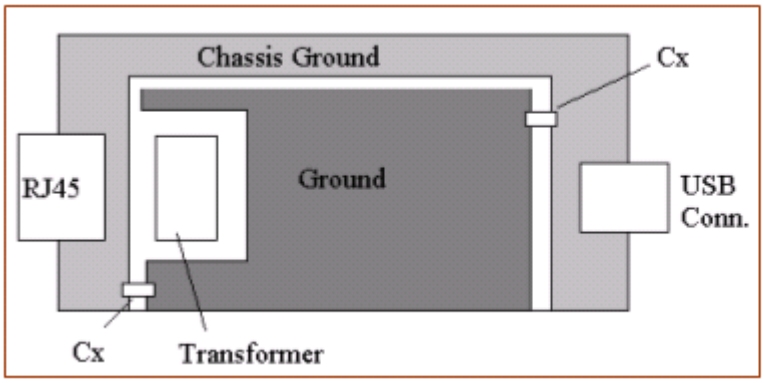


Figure 13 Correct placement of power and ground planes

- If you use a permanently attached cable (plus the shield wire).it may require additional filtering for FCC test pass.and the length of unshielded cable should be limited to 3cm or less.

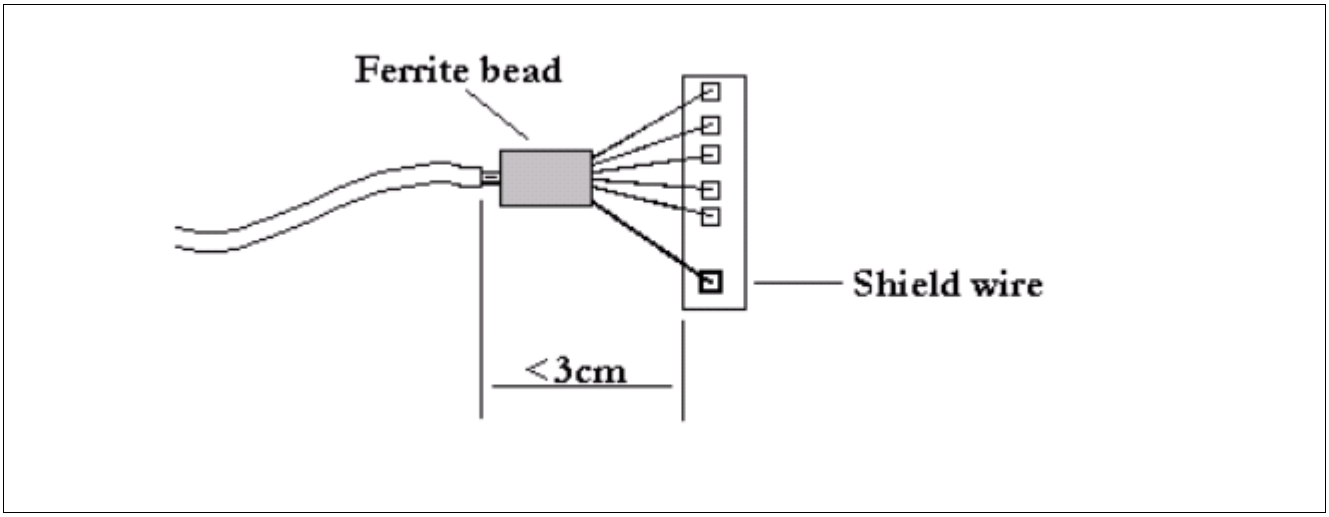


Figure 14 Limited length of unshielded cable

- Please connect pin12(GndRef) and pin8(GndR) first then use signal via to Gnd.

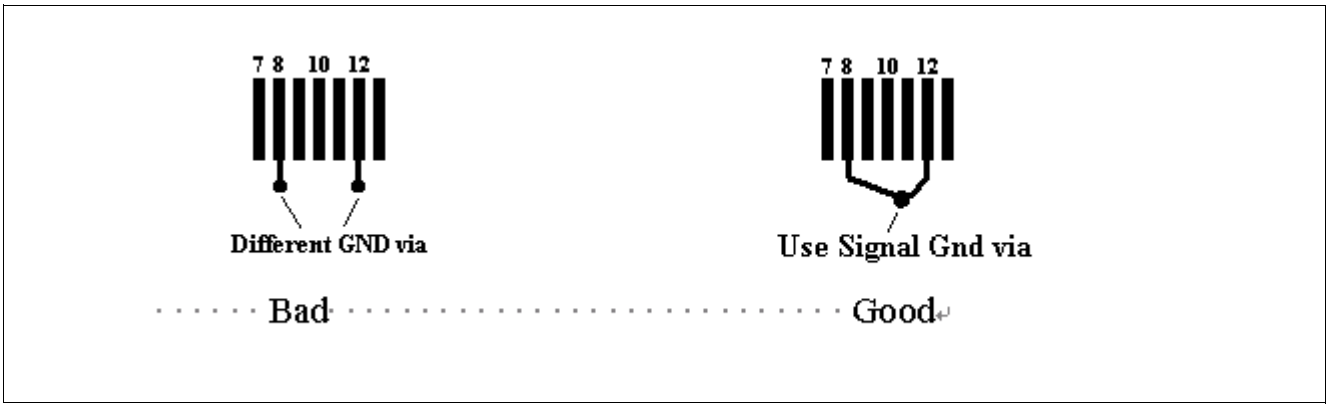


Figure 15 Connection of pin12(GndRef) and pin8(GndR)

8 APPENDIX 2 - EEPROM Interface & Example

8.1 General EEPROM Format Description

If the EEPROM contents from offset 0 to offset 5 is "FF_FF_FF_FF_FF_FF", it means the EEPROM isn't programmed correctly, The default values for every field are used instead of loading from EEPROM.

Table 38 General EEPROM Format Description

Offset(byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2nd byte of Ethernet node ID.
02	node_id2	The 3rd byte of Ethernet node ID.
03	node_id3	The 4th byte of Ethernet node ID.
04	node_id4	The 5th byte of Ethernet node ID.
05	node_id5	The 6th byte of Ethernet node ID.
06-07	reserved	
08	max_pwr	The maximum USB power consumption.
09	ep3_interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	iso_enable	0
0A[1]	USB transceiver Test_mode	0: select external USB transceiver. 1: select internal USB transceiver.
0A[4:2]	MII Test_mode	000b: tri-state MII pins 001b: enable MAC's MII signals to external interface 010b: enable PHY's MII signals to external interface 011b: monitor MII mode
OA[7]	Remote wakeup Enable	0: Enable 1: Disable
0B[7:6]	LED mode	Refer to pin assignment
0B[5:0]	reserved	
0C	languageid_lo	The low byte of language ID.
0D	languageid_hi	The high byte of language ID.
0E-0F	reserved	
10	manuid_lo	The low byte of manufacture ID.
11	manuid_hi	The high byte of manufacture ID.
12	proid_lo	The low byte of product ID.
13	proid_hi	The high byte of product ID.
14	manu_str_len	The length for manufacture string.
15	manu_str_offset	The word offset address of manufacture string.
16	pro_str_len	The length for product string.
17	pro_str_offset	The word offset address of product string.

Table 38 General EEPROM Format Description (cont'd)

Offset(byte)	Field	Description
18	seri_str_len	The length for serial number string
19	seri_str_offset	The word offset address of serial number string.

8.2 Example

Table 39 Example 1

offset(byte)	value
0000h	00, 00 E8 00 02 2C 00 00
0008h	50 01 02 00 09 04 00 00
0010h	A6 07 11 85 0E 10 2A 20
0018	0A 38 00 00 00 00 00 00
0020	0E 03 41 00 44 00 4D 00
0028	74 00 65 00 6B 00 00 00
0030	1E 00 55 00 53 00 42 00
0038	20 00 31 00 30 00 2F 00
0040	2A 03 55 00 53 00 42 00
0048	20 00 54 00 6F 00 20 00
0050	4C 00 41 00 4E 00 20 00
0058	43 00 6F 00 6E 00 76 00
0060	65 00 72 00 74 00 65 00
0068	72 00 00 00 00 00 00 00
0070	0A 03 30 00 30 00 30 00
0078	31 00 00 00 00 00 00 00

Table 40 Example 2

Offset(byte)	Value	Description
00-05	00_00_E8_10 _46_02	NIC node ID
08	50	maximum power 160mA
09	01	interrupt endpoint 3 polling interval 1ms
0A	02	isochronous endpoint disable, select internal USB transceiver Use internal Ethernet PHY Wake on Lan enable
0C-0D	0904	Language ID 0409
10-11	A607	manufacture ID 07A6
12-13	8511	product ID 8511
14	0E	manufacture string length 0E bytes
15	10	manufacture string starts from word offset 10h, thus byte offset 20h.
16	1E	product string length 1E bytes

Table 40 Example 2

Offset(byte)	Value	Description
17	18	product string starts from word offset 18h, thus byte offset 30h.
18	0A	serial number string length 0A bytes
19	38	serial number string starts from word offset 38h, thus byte offset 70h.
20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string
30-4E	1E 03 55 00 53 00 42 00 20 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 00 31 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

9 APPENDIX 3 - USB Device Operation

9.1 Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal registers setting are also via this endpoint. The response to each command is described in section 7.

9.2 Endpoint 1 bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64-byte USB packets on USB. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint if RX FIFO is either full or any packet is inside, the data in RX FIFO is returned in USB data stage. If ACK is received from USB host, data in RX FIFO is flushed. If no response or NAK is received from USB host, the content in RX FIFO will be re-transmitted. If RX FIFO isn't ready for transmission, NAK is returned to USB host.

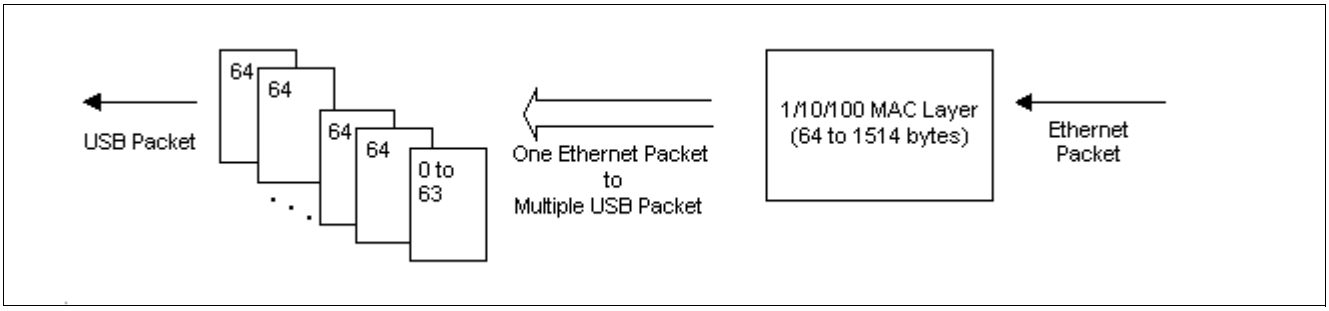


Figure 16 Transmission of RX FIFO

The received status is reported as follows:

Table 41 Received status

Offset	Bit	Field	Description
Offset0	7-0	rx_bytecnt_lo	The received byte count[7:0].
Offset1	3-0	rx_bytecnt_hi	The received byte count[11:8].
	7-4	reserved	
Offset2	0	Multicast_frame	Indicate receive a multicast frame.
	1	Long_pkt	Indicate received packet length > 1518 bytes
	2	Runt_pkt	Indicate received packet length < 64 bytes.
	3	crc_err	Indicate CRC check error.
	4	Dribble_bit	Indicate packet length is not integer multiple of 8-bit.
	7-5	reserved	
Offset3	7-0	reserved	

9.3 Endpoint 2 bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated as multiple 64-byte USB packets on USB. The first two bytes in every first concatenated USB packet indicate the total length of the Ethernet packet. The end of the Ethernet packet is indicated with less then 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage is transferred to TX FIFO when TX FIFO is free and ACK is returned. If TX FIFO isn't free, NAK is returned.

Table 42 Endpoint 2 bulk OUT

Field	1st byte in 1st USB packet	2nd byte in 1st USB packet	The following packets
Content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet

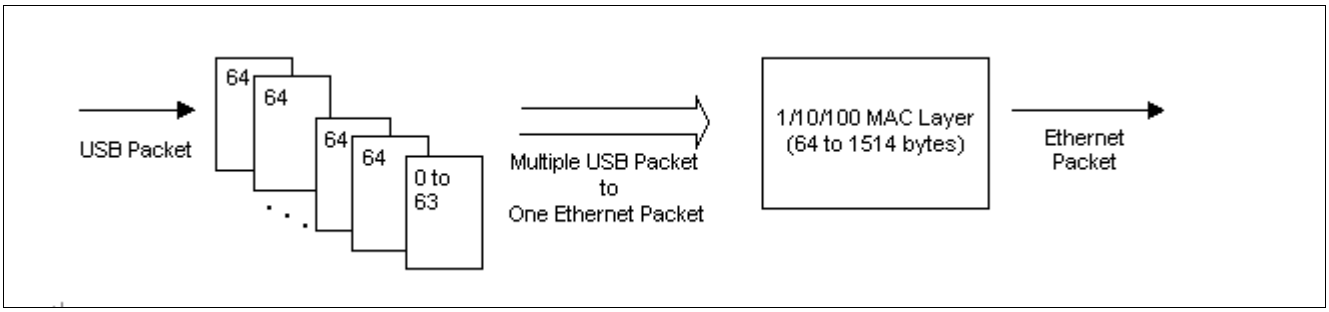


Figure 17 Sending the USB packet to Ethernet

9.4 Endpoint 3 interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

Table 43 Endpoint 3 interrupt IN

Offset0	Offset1	Offset2	Offset3	Offset4	Offset5	Offset6-7 (2B)
tx_status(Reg 2Bh)	tx_status(Reg 2Ch)	rx_status(Reg 2Dh)	rx_lostpkt(Reg2Eh)	rx_lostpkt(Reg2Fh)	Wakeup_status(Reg7Ah)	0

10 APPENDIX 4 - USB Command

- Get_Register (Vendor Specific) Single/Burst read

Table 44 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
C0	F0	0	{RegIndex[0:7], 00}	length

Table 45 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1)	{RegIndex+2)

The returned total number of registers depends on the length field.

- Set_Register (Vendor Specific) Single write

Table 46 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	{value[0:7],mask[0:7]}	{RegIndex[0:7], 00}	1

- Set_Register(Vendor Specific) Burst write

Table 47 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	0	{RegIndex[0:7], 00}	length

Table 48 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1)	{RegIndex+2)	{RegIndex+3}

Ex. Write 44 to RegIndex=05h, the transfer will be

Table 49 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	4400	0500	0100

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported => DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex=07h and data from 01d to 20d

Table 50 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	0000	0700	1400

Table 51 Data Stage - 1st OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

Table 52 Data Stage - 2nd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	02	0A	0B	0C	0D	0E	10

Table 53 Data Stage - 3rd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

- Get_Status(Device)

Table 54 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	0	0	0	2

Table 55 Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]:Self Powered
0	Register of remote_wakeup	1

- Get_Status(Interface)

Table 56 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	0	0	0	2

Table 57 Data Stage

D[15:0]
0

- Get_Status(EP0)

Table 58 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0080 or 0000	2

Table 59 Data Stage

D[15:1]	D[0]: Halt
0	register of ep0_halt

- Get_Status(EP1) bulk IN

Table 60 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0081	2

Table 61 Data Stage

D[15:1]	D[0]: Halt
0	register of ep1_halt

- Get_Status(EP2) bulk OUT

Table 62 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0002	2

Table 63 Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

- Get_Status(EP3) interrupt IN

Table 64 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0083	2

Table 65 Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

- Get_Descriptor(Device) total 18-byte

Table 66 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0001	0	length

Table 67 Data Stage: wLength field specifies the total byte count to return (1)

Offset0	Offset1(type)	Offset2(USB release no.)	Offset4(Class code)	Offset5(Sub Class Code)	Offset6(Protocol)	Offset7(EP0 MaxPktSize)	Offset8 (vendor ID)
12(1B)	01(1B)	0110(2B)	00(1B)	00(1B)	00(1B)	8(1B)	(2B)

Table 68 Data Stage: wLength field specifies the total byte count to return (2)

Offset10 (productID)	Offset12(releaseID)	Offset14 (manufacture)	Offset15 (Product)	Offset16(serial no.)	Offset17(no. of config)
(2B)	0001(2B)	01(1B)	02(1B)	03(1B)	01(1B)

- Get_Descriptor(Configuration) total 39-byte

Table 69 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0002	0	length

Table 70 Setup Stage - Configuration Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (TotalLength)	Offset4 (NumInterface)	Offset5 (ConfgValue)	Offset6 (StringIndex)	Offset7 (Attribute)	Offset8 (MaxPower)
09(1B)	02(1B)	0027(2B)	01(1B)	00(1B)	00(1B)	E0(1B)	max_pwr(1B)

Table 71 Setup Stage - Interface 0 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (InterfaceNum)	Offset3 (AltInterface)	Offset4 (NumEP)	Offset5 (IntfClass)	Offset6 (IntfSubClass)	Offset7 (IntfProtocol)	Offset8 (StringIndex
09(1B)	04(1B)	00(1B)	00(1B)	04(1B)	xx(1B)	E0(1B)	xx(1B)	00(1B)

Table 72 Setup Stage - FEP1 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	81(1B)	02(1B) bulk	0064(2B)	00(1B)

Table 73 Setup Stage - FEP2 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	02(1B)	02(1B) bulk	0064(2B)	00(1B)

Table 74 Setup Stage - FEP2 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	83(1B)	03(1B) interrupt	0008(2B)	p3_interval(1B)

- Get_Descriptor(String) Index0, LanguageID Code

Table 75 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0003	0000	length

Table 76 Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID)
04(1B)	03(1B)	0904(2B)

- Get_Descriptor(String) Index1, manufacture

Table 77 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0103	0904	length

Table 78 Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

- Get_Descriptor(String) Index2, product

Table 79 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0203	0904	length

Table 80 Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

- Get_ Descriptor(String) Index3, serial no.

Table 81 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0303	0904	length

Table 82 Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

- Get_Configuration

Table 83 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	08	0	0	0001

Table 84 Data Stage

Offset0 (ConfgValue)(1B)

- Get_Interface

Table 85 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	10	0	0	0001

Table 86 Data Stage

Offset0 (AltIntf)(1B)
00

- Set_Address
- Set_Configuration
- Set_Interface
- Clear_Feature(Device) Remote Wakeup

Table 87 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	01	0100	0	0

- Set_feature(Device) Remote Wakeup

Table 88 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	03	0100	0	0

- Clear_Feature(EP0,1,2,3) Halt

Table 89 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

- Set_Feature(EP0,1,2,3) Halt

Table 90 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

11 APPENDIX 5 - Design Notes for Ethernet & MII Application(HPNA&HomePlug)

11.1 48MHz Crystal

ADM8511/X need a 48 MHz crystal (+/- 50ppm,over tone) to work on USB side. Because the 48 MHz crystal is a over tone part, It need work with a L/C pair. However, 48 MHz fundamental crystal is also valid and associates with two ceramic capacitor.

11.2 SRAM

All of the SRAM pin can be NC (No Connection).

11.3 RST# and POREN_N

- Internal Power On Reset in ethernet only or combo (Ethernet & HPNA) solution: The ADM8511/X provides internal power reset. In ethernet only or combo solution, you can let RST# and POREN_N pin NC.
- External reset in external PHY only solution.(e.g. Home PNA only) Condition: (1) POREN_N pull to high and (2) RST# asserts low when external reset is active.

RST# combines with a reset circuit (e.g. RC circuit) to provide a low pulse to be reset signal. The duration of the low pulse is 50ms at least. The recommended time is more than 80ms. Moreover, it still needs 25MHz crystal oscillation circuit and Ribb pin connects a 10K resistor to ground.

11.4 XLNKSTS

1. Ethernet only solution: This pin need strapping to low directly
2. Combo or External PHY only solution: reports link status information to system and level change trigger.

11.5 LED

All of the LED pin are active Low and only display internal PHY status.

11.6 Ethernet pin (LED,XTLP/N,TXOP/N,RXIP/N,RIBB,TST0.....K3

In External PHY solution, All can be NC.

11.7 MII interface signal pins

- In ethernet only solution: All of the MII pin can be NC.
- In combo or external PHY only solution
  - MDIO requires external 1.5k pull-up resistor.
  - TXEN requires external 4.7k pull-down resistor. If the external PHY did not provide RXER, this pin needs strapping to low directly.

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